MOTOROLA

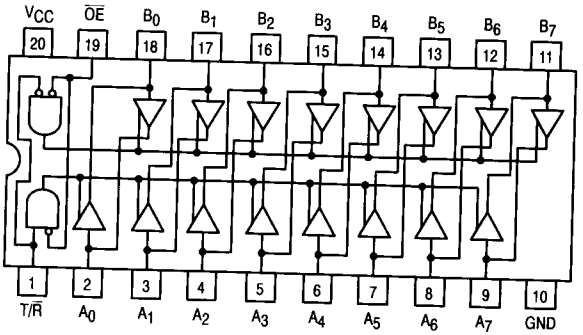
Octal Bus Transceivers With 3-State Outputs (Non-Inverting)

ELECTRICALLY TESTED PER:
MIL-M-38510/34803

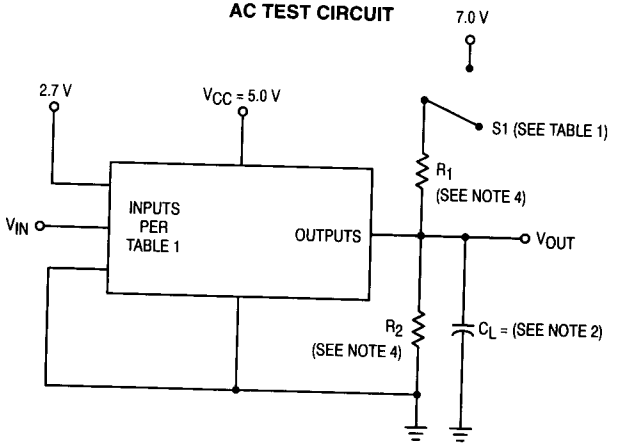
The 54F245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a high-Z condition.

- Non-Inverting Buffers
- Bidirectional Data Path
- B Outputs Sink 64 mA
- MOS Compatible

LOGIC DIAGRAM



AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 4-120

Military 54F245

AVAILABLE AS:

1) JAN: JM38510/34803BXA
2) SMD: 8551101
3) 883: 54F245/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$T/\overline{R}$	1	1	1	V_{CC}
A_0	2	2	2	OPEN
A_1	3	3	3	OPEN
A_2	4	4	4	OPEN
A_3	5	5	5	OPEN
A_4	6	6	6	OPEN
A_5	7	7	7	OPEN
A_6	8	8	8	OPEN
A_7	9	9	9	OPEN
GND	10	10	10	GND
B_7	11	11	11	OPEN
B_6	12	12	12	OPEN
B_5	13	13	13	OPEN
B_4	14	14	14	OPEN
B_3	15	15	15	OPEN
B_2	16	16	16	OPEN
B_1	17	17	17	OPEN
B_0	18	18	18	OPEN
$\overline{OE}$	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Inputs		Output
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level

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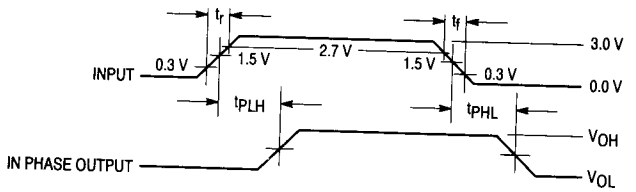
Table 1

Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



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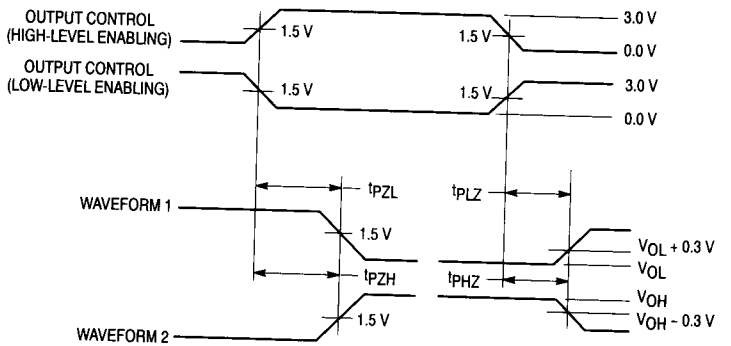
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



NOTES:

1. V_{IN} = input pulse and has the following characteristics: PRR = 1.0 MHz, $t_r = t_f \leq 2.5$ ns.
2. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance without package in test fixture.
3. Voltage measurements are to be made with respect to network ground terminal.
4. $R_1 = R_2 = 500\ \Omega \pm 5.0\%$.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IH} = 2.0V (other inputs are open), T/$\overline{R}$ = 2.0 V, $\overline{OE}$ = 0.8 V.
V_{OL}	Logical "0" Output Voltage		0.55		0.55		0.55	V	V_{CC} = 4.5 V, I_{OH} = 48 mA, V_{IL} = 0.8V (other inputs are open), T/$\overline{R}$ = 2.0 V, $\overline{OE}$ = 0.8 V.
V_{OH1}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V, I_{OH} = −12 mA, V_{IH} = 2.0 V (other inputs are open), T/$\overline{R}$ = 2.0 V, $\overline{OE}$ = 0.8 V.
V_{OH2}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OL} = −1.0 mA, V_{IH} = 2.0 V (other inputs are open), T/$\overline{R}$ & $\overline{OE}$ = 0.8 V.
V_{OL1}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V (other inputs are open), T/$\overline{R}$ & $\overline{OE}$ = 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, $\overline{OE}$ = 0 V, all other inputs are open, T/$\overline{R}$ = 5.5 V or 0 V.
I_{IH1}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IH2}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IH} = 7.0 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		1.0		1.0		1.0	mA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, T/$\overline{R}$ = 5.5 V or 0 V, other inputs are open, $\overline{OE}$ = 0 V.
I_{IL1}	Logical "0" input Current	−0.04	−1.2	−0.04	−1.2	−0.04	−1.2	mA	V_{CC} = 5.5 V, $\overline{OE}$ = 0.5 V, T/$\overline{R}$ = 0 V, other inputs are open.
I_{IL2}	Logical "0" Input Current	−0.04	−1.2	−0.04	−1.2	−0.04	−1.2	mA	V_{CC} = 5.5 V, T/$\overline{R}$ = 0.5 V, $\overline{OE}$ = 0 V, other inputs are open.
I_{OSH}	Output Short Circuit Current B Side	−100	−325	−100	−325	−100	−325	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (other inputs are open), V_{OUT} = 0 V, T/$\overline{R}$ = 5.5 V, $\overline{OE}$ = 0 V.
I_{OSL}	Output Short Circuit Current A Side	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (other inputs are open), V_{OUT} = 0 V, T/$\overline{R}$ = 0 V, $\overline{OE}$ = 0 V.
I_{IOZH}	Output Off Current High		70		70		70	µA	V_{CC} = 5.5 V, V_{IL} = 0 V, V_{IH} = 5.5 V, $\overline{OE}$ = 2.0 V, T/$\overline{R}$ = 0 V or 5.5 V.
I_{IOZL}	Output Off Current Low	−0.04	−1.2	−0.04	−1.2	−0.04	−1.2	mA	V_{CC} = 5.5 V, V_{IL} = 0.5 V, V_{IH} = 5.5 V, $\overline{OE}$ = 2.0 V, T/$\overline{R}$ = 5.5 V or 0 V.
I_{CCH}	Power Supply Current		110		110		110	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{OE}$ = 0 V, T/$\overline{R}$ = 5.5 V or 0 V.
I_{CCL}	Power Supply Current		130		130		130	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs), $\overline{OE}$ = 0 V, T/$\overline{R}$ = 5.5 V or 0 V.
I_{CCZ}	Power Supply Current Off		143		143		143	mA	V_{CC} = 5.5 V, all inputs are open, $\overline{OE}$ = 5.5 V, T/$\overline{R}$ = 5.5 V or 0 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	− 55°C		
		Subgroup 7	Subgroup 8A	Subgroup 8B		
	Functional Tests					per Truth Table with V_{CC} = 4.5 V, (**Repeat at**), V_{CC} = 5.5 V, V_{INL} = 0.5 V, V_{INH} = 2.4 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output Output High-Low	1.5	6.5	1.0	8.0	2.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output Output Low-High	1.5	6.0	1.0	8.0	1.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLH2}	Propagation Delay /Data-Output Output Low-High	1.5	6.0	1.0	8.0	1.0	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHL2}	Propagation Delay /Data-Output Output High-Low	1.5	6.5	1.0	8.5	1.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0	6.5	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLZ2}	Propagation Delay /Data-Output	2.0	6.5	2.0	10	2.0	10	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0	6.5	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHZ2}	Propagation Delay /Data-Output	2.0	6.5	2.0	9.0	2.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZL1}	Propagation Delay /Data-Output Output Low-High	2.5	10	2.0	13	2.0	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZL2}	Propagation Delay /Data-Output	2.5	10	2.0	13	2.0	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZH1}	Propagation Delay /Data-Output Output Low-High	2.5	8.5	2.0	11	2.0	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZH2}	Propagation Delay /Data-Output	2.5	8.5	2.0	11	2.0	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, $R_1 = R_2$ = 500 Ω.