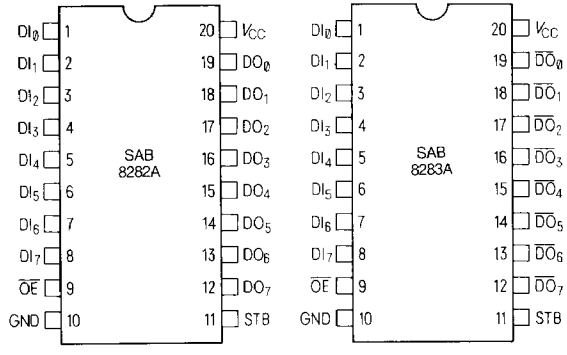
SIEMENS

Preliminary

# SAB 8282A/SAB 8283A Octal Latch

- Fully compatible with SAB 8282/SAB 8283
- 40% Less Power Supply Current than Standard SAB 8282/SAB 8283
- Address Latch for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus
- Fully Parallel 8-Bit Data Register and Buffer
- No Output Low Noise when Entering or Leaving High Impedance State
- 3-State Outputs
- Transparent during Active Strobe
- 20-Pin Package

**Pin Configuration**



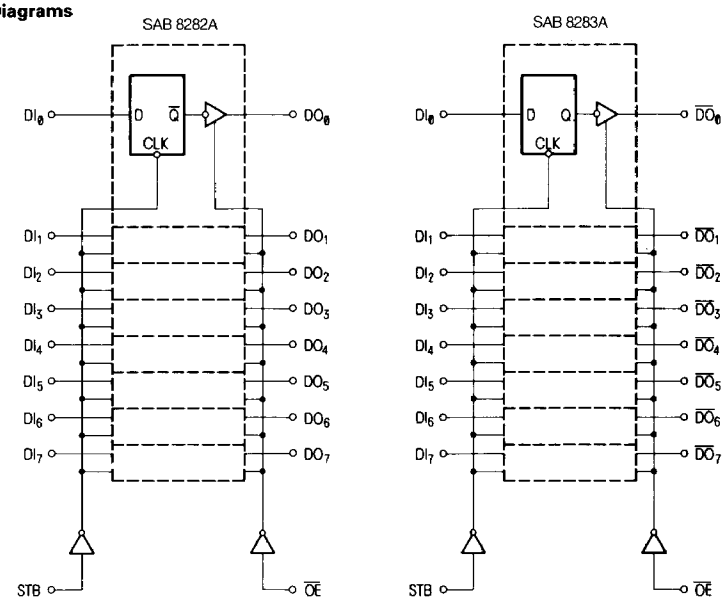

**Pin Names**

| | |
|---|---|
| $DI_0 - DI_7$ | Data In |
| $DO_0 - DO_7$ | Data Out |
| $\overline{OE}$ | Output Enable |
| STB | Strobe |
| $V_{CC}$ | Power Supply (+5V) |
| GND | Ground (0V) |

The SAB 8282A and SAB 8283A are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The SAB 8283A inverts the input data at its outputs while the SAB 8282A does not.

Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

**Logic Diagrams**




## Pin Definitions and Functions

| Symbol | Number | Input (I) Output (O) | Function |
|---|---|---|---|
| STB | 11 | I | STROBE – STB is an input control pulse used to strobe data at the data input pins ($A_0$–$A_7$) into the data latches. This signal is active HIGH to admit input data. The data is latched at the HIGH to LOW transition of STB. |
| $\overline{OE}$ | 9 | I | OUTPUT ENABLE – $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches onto the data output pin ($DO_0$–$DO_7$ or $\overline{DO_0}$–$\overline{DO_7}$). $\overline{OE}$ being inactive HIGH forces the output buffers to their high impedance state. |
| $DI_0$–$DI_7$ | 1–8 | I | DATA INPUT PINS – Data presented at these pins satisfying setup time requirements when STB is strobed and latched into the data input latches. |
| $DO_0$–$DO_7$ (SAB 8282A) $\overline{DO_0}$–$\overline{DO_7}$ (SAB 8283A) | 12–19 | O | DATA OUTPUT PINS – When $\overline{OE}$ is true, the data in the data latches is presented as inverted (SAB 8283A) or non-inverted (SAB 8282A) data onto the data output pins. |
| $V_{CC}$ | 20 | – | Power Supply (+5V) |
| GND | 10 | – | Ground (0V) |

## Functional Description

The SAB 8282A and SAB 8283A octal latches are 8-bit latches with 3-state output buffers.
Data having satisfied the setup time requirements is latched into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent.

Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

## Absolute Maximum Ratings[1)]

| | |
|---|---|
| Temperature Under Bias | 0 to +70°C |
| Storage Temperature | −65 to +150°C |
| All Output and Supply Voltages | −0.5 to +7V |
| All Input Voltages | −1.0 to +5.5V |
| Power Dissipation | 1W |

## D. C. Characteristics

$T_A$ = 0 to 70°C; $V_{CC}$ = +5V ±10%

| Symbol | Parameter | Limit Values | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $V_C$ | Input Clamp Voltage | | −1 | V | $I_C$ = −5 mA |
| $I_{CC}$ | Power Supply Current<br>SAB 8282A<br>SAB 8283A | – | <br>100<br>90 | mA | all outputs open |
| $I_F$ | Forward Input Current | – | −0.2 | | $V_F$ = 0.45V |
| $I_R$ | Reverse Input Current | | 50 | µA | $V_R$ = 5.25V |
| $V_{OL}$ | Output LOW Voltage | | 0.45 | V | $I_{OL}$ = 32 mA |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | – | | $I_{OH}$ = −5 mA |
| $I_{OFF}$ | Output Off Current | – | ±50 | µA | $V_{OFF}$ = 0.45 to 5.25V |
| $V_{IL}$ | Input LOW Voltage | | 0.8 | V | $V_{CC}$ = 5.0V [2)] |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | – | | |
| $C_{IN}$ | Input Capacitance | – | 12 | pF | $F$ = 1 MHz<br>$V_{BIAS}$ = 2.5V, $V_{CC}$ = 5V<br>$T_A$ = 25°C |

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Output Loading: $I_{OL}$ = 32 mA; $I_{OH}$ = −5 mA; $C_L$ = 300 pF

## A.C. Characteristics

$T_A$ = 0 to +70°C; $V_{CC}$ = +5 V ± 10%

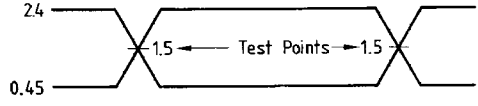
**Loading**

Outputs: $I_{OL}$ = 32 mA; $I_{OH}$ = −5 mA; $C_L$ = 300 pF

| Symbol | Parameter | Limit Values | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $t_{IVOV}$ | Input to Output Delay<br>–Inverting<br>–Non-Inverting | <br>5<br>5 | <br>22<br>30 | ns | 2) |
| $t_{SHOV}$ | STB to Output Delay<br>–Inverting<br>–Non-Inverting | <br>10<br>10 | <br>40<br>45 | | |
| $t_{EHOZ}$ | Output Disable Time | 5 | 18 | | |
| $t_{ELOV}$ | Output Enable Time | 10 | 30 | | |
| $t_{IVSL}$ | Input to STB Setup Time | 0 | – | | |
| $t_{SLIX}$ | Input to STB Hold Time | 25 | | | |
| $t_{SHSL}$ | STB HIGH Time | 15 | | | |
| $t_{ILIH}$, $t_{OLOH}$ | Input, Output Rise Time | – | 20 | | From 0.8 to 2.0 V |
| $t_{IHIL}$, $t_{OHOL}$ | Input, Output Fall Time | | 12 | | From 2.0 to 0.8 V |

## A.C. Testing Input, Output Waveform

**Input/Output**

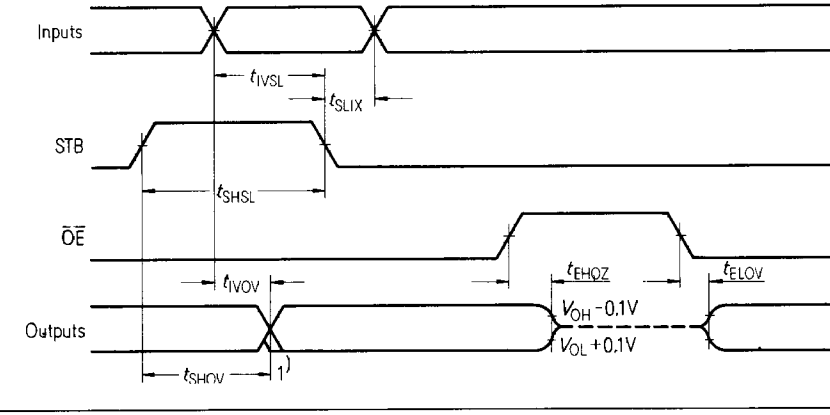



A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 1.5 V for both a logic "1" and "0".

## Waveforms

All timing measurements are made at 1.5 V unless otherwise noted.

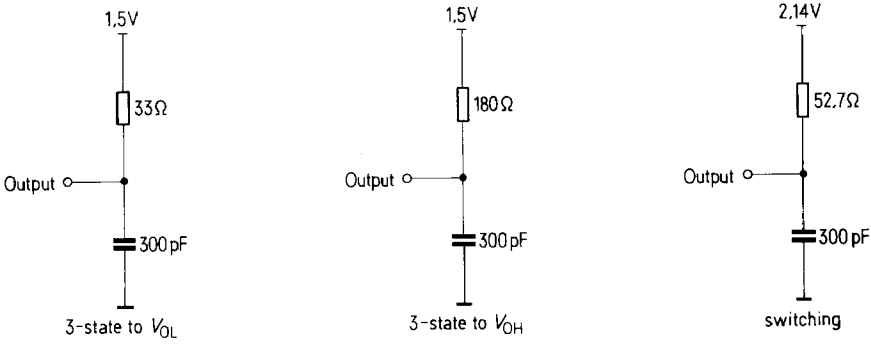
**Timing**



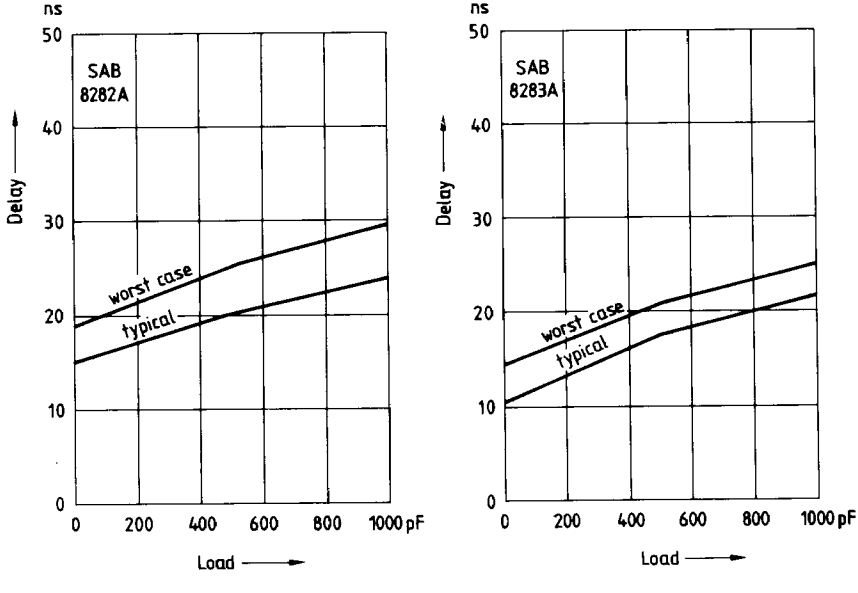

1) SAB 8283A Only – Output may be momentarily invalid following the high going STB transition.

2) See waveforms and test load circuit.

**Output Test Load Circuits**




**Output Delay vs. Capacitance**



## Ordering Information

| Type | Description | Ordering code |
|---|---|---|
| SAB 8282A–P | Octal Latch, non inverting (plastic) | Q 67020–Y149 |
| SAB 8283A–P | Octal Latch, inverting (plastic) | Q 67020–Y150 |