VSC7395

Enhanced 5 + 1-Port Integrated Gigabit Ethernet Switch with Transceivers

Datasheet

VMDS-10193
Revision 4.1
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Confidential

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Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.1

Revision 4.1 of this datasheet was published in July 2006. The following is a summary of the changes implemented in the datasheet:

- The section about IP Multicast Groups was modified due to improvements concerning IPMC address changes to the MAC table. For more information, see "IP Multicast Groups," page 81.
- The REVISION_NUMBER for the device was changed. For more information, see Table 77, page 152.
- The SI_DO is not driven during reset; therefore, information about this issue was removed from the Design Guidelines. For more information, see "SI," page 286.
- Minor design improvements for this revision resolved an issue about excessive collisions being counted incorrectly. This issue was removed from the Design Considerations section.

Revision 4.0

Revision 4.0 of this datasheet was published in May 2006. The following is a summary of the changes implemented in the datasheet:

- The VSC7395-03 devices with extended temperature ranges are now available. Information about the extended temperature devices was added throughout the datasheet.
- Information was added throughout the datasheet, especially in the V-Core CPU section, to clarify the configurations for the ICPU_PI_En and ICPU_SI_Boot_En pins.
- The information about the various clock settings for CLK_SEL in the MAC configuration register was modified to clarify the possible settings for a particular PHY interface.
- The rate of broadcasts, multicasts, and unicasts allowed for flooding storm control was updated.
- The REVISION_NUMBER for the PHY identifier number 2 was updated.
- The value for input high voltage, V_{IH}, was changed from 2.0 V to 2.1 V for the DC specifications for RefClk and the DC specifications for PI, V-Core CPU, SI, JTAG, and other control signals.
- The value for input high voltage, V_{IH}, was changed from 1.7 V to 2.0 V for the DC specifications for MII and GMII using 3.3 V power supply.
- The specification for output leakage, I_{OZ}, was added to the datasheet.
- The maximum operating current values were modified for I_{DD_IOMAC} (the operating current for V_{DD_IOMAC}).
- In the AC specifications for the crystal option, the maximum value for the equivalent series resistance of crystal was added.
- More information and several values for the AC specifications for RGMII in compensated mode were added.

- The values for the stress ratings were added, including the electrostatic discharge (ESD) classification.
- The thermal diode information was updated.
- Information about the MSL value was updated.

Revision 2.1

Revision 2.1 of this datasheet was published in December 2005. The following is a summary of the changes implemented in the datasheet:

- Serial LED data is clocked out on the falling edge. LED_CLK in the diagrams for Serial LED Output Functional Timing and Serial LED Output AC Timing was inverted to reflect this. The LED_DATA propagation delay, t_{pd}, was updated with a minimum value of –15 ns and a typical value of 0 ns in the table for Serial LED Output Timing.
- In the Frame Classes table, the DMAC value for IGMP, IP Multicast Data, and IP Multicast Ctrl was updated.
- Information about updating IPMC entries in the MAC table was added.
- The initialization sequence was modified.
- MEMRES was removed from this datasheet.
- Aging information for the TIMECMP register was updated.
- The value for the MODEL_NUMBER was updated.
- Information about controlling the amplitude of the 1000BASE-T signal waveform was added to the DACG_AMPLITUDE_1000BT_CFG bit in the PHY_CTRL_EXT3 register.
- The values for the maximum operating current, the typical current consumption, and the maximum power consumption were updated.
- For the MII Management AC specifications, the values for MDIO setup to MDC on write, $t_{su(W)}$, and MDIO hold from MDC on write, $t_{h(W)}$, were updated.
- For the serial interface AC specifications, the minimum values for DI hold from clock, $t_{h(DI)}$, and the enable inactive after clock (input cycle), t_{lag1}, were updated.
- For the parallel interface AC specifications, the minimum value for Addr, Data, nWR hold from nCS low, t_h, and the maximum value for data disable time from either nCS or nOE high, $t_{dis(E)}$, were updated.
- For the V-Core CPU RAM read and write specifications, the minimum value for address hold from RAM chip select, $t_{h(A)}$, was updated. For the V-Core CPU ROM/Flash read and Flash write specifications, the minimum value for address hold from ROM chip select, $t_{h(A)}$, was updated.
- For the JTAG AC specifications, the value for JTAG TDO hold from TCK falling, $t_{h(TDO)}$, was updated.
- The value for θ_{JC} was updated.
- Thermal diode information was added.
- Reverse MII information was added.
- More information about the SI_DO pin was added to the Design Guidelines.
- Product errata was added.

Revision 2.0

Revision 2.0 of this datasheet was published in October 2005. This was the first publication of the document.

1 Introduction

This datasheet provides information and specifications for the VSC7395, an enhanced 5 + 1-port integrated Gigabit Ethernet switch with transceivers.

1.1 Notations

Notations used throughout the datasheet are defined here.

1.1.1 RS-232 and UART Terminology

The commonly used term, RS-232, is used to define an LVTTL-compliant UART interface throughout this datasheet.

1.1.2 Register and Field Notation

This datasheet uses the following register and field notation:

<BLOCK>::<SUBBLOCK>::<FIELD>

In sections where only one block is discussed or the register has already been placed in a specific target, the <BLOCK> may be omitted for brevity:

<SUBBLOCK>::<FIELD>

1.2 Standard References

This datasheet uses the following industry references.

1.2.1 References for the Ethernet Port

The Ethernet ports have been designed to meet or exceed the requirements found in the following standards:

- IEEE Std 802.3-2002 Edition for Ethernet, Fast Ethernet and Gigabit Ethernet
- Power-over-Ethernet IEEE Std 802.3af
- Cisco Systems Serial-GMII specification, version 1.7

1.2.2 References for Packaging

Packaging references the JEDEC standard IPC/JEDEC-J-STD-020.

2 Product Overview

SparX-G5e is a full-featured, 5+1 port, Gigabit Ethernet switch-on-a-chip with five integrated tri-speed copper transceivers, one tri-speed RGMII/GMII, and several integrated management interfaces.

SparX-G5e provides nonblocking, wire-speed Gigabit performance on all ports and has been optimized for SMB and SOHO for unmanaged, as well as managed, applications. SparX-G5e does not require external memory, because internal memory buffers are sufficient to absorb substantial bursts.

Web-based and SNMP management are made possible through the optionally enabled on-chip 8051 CPU or through the faster 8-bit parallel interface. In addition, less processor-intensive, managed operation can be achieved using a simple four-wire serial interface.

The SparX-G5e device supports programmable higher layer classification and prioritization to enable enhanced Quality of Service (QoS) support for real-time applications such as VoIP.

The following features are highlights of the SparX-G5e device.

- 5+1 Gigabit Ethernet ports with nonblocking wire-speed performance
- Five tri-speed (10/100/1000 Mbps) copper transceivers (IEEE Std 802.3ab-compliant)
- One tri-speed RGMII/GMII
- Choice of on-chip 8051 CPU or off-chip 8-bit CPU for SNMP and Web-based management
- On-chip CPU booting through serial EEPROM
- Supports both wire-speed automatic learning and CPU-based learning
- 136 kilobytes on-chip frame buffer
- 8,192 MAC addresses and 4,096 VLAN support (IEEE Std 802.1Q)
- 8,192 IP multicast groups supported
- Jumbo frame support at all speeds (10/100/1000 Mbps)
- Programmable multi-layer classifier with four QoS classes
- Strict or weighted fairness queueing with guaranteed bandwidth allocation
- DSCP (IPv4 and IPv6) and IEEE Std 802.1p support
- DSCP remarking for both IPv4 and IPv6 packets
- Provider Bridging support with multiple VLAN tags (Q-in-Q)
- Broadcast and multicast storm control
- Full-duplex flow control (IEEE Std 802.3x) and half-duplex back pressure
- Link aggregation support based on Layer 2–4 information (IEEE Std 802.3ad)
- Rapid Spanning Tree Protocol support (IEEE Std 802.1w)
- Multiple Spanning Tree support (IEEE Std 802.1s)
- Port-based access control support (IEEE Std 802.1X)
- IGMP, GARP, GMRP, and GVRP support
- Royalty-free web-managed software stack available from Vitesse
- Vitesse VeriPHY™ Cable Diagnostics

2.1 Functional Overview

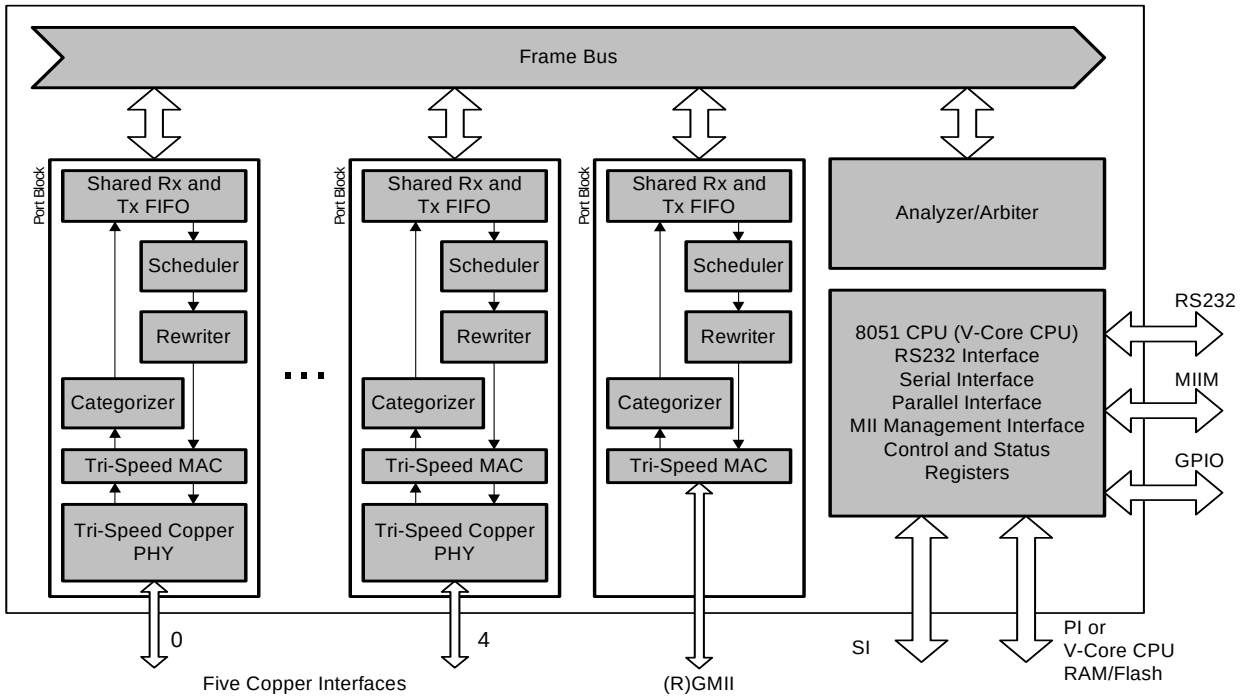
SparX-G5e is a 5+1 × tri-speed Ethernet Switch-on-a-Chip with five integrated copper transceivers and one tri-speed RGMII/GMII. It provides non-blocking wire-speed performance using an internal 20-Gbps frame bus.

SparX-G5e can operate as either a VLAN-aware switch or a VLAN-unaware switch. It can forward frames at Layer 2, based on information from Layer 2 and Layer 3. All memory is included on-chip, because each port has its own shared memory of 20 kilobytes for frame storage.

This section gives an overview of the functionality and features of SparX-G5e. For more information, see "Functional Descriptions," page 37.

An overall block diagram of SparX-G5e device is shown in the following figure.

Figure 1. Functional Block Diagram



2.1.1 Tri-Speed Gigabit Copper PHYs

SparX-G5e implements 5 separate low-power tri-speed Ethernet copper PHYs, providing support for full-duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps. The PHYs leverage Vitesse's fourth generation SimpliPHY™ DSP Technology that yields industry-leading performance and total switch + PHY power consumption of less than 600 mW per port.

The VeriPHY™ Link Management and Cable Diagnostics Suite can be used with each of SparX-G5e's 5 built-in PHYs. VeriPHY provides network and cable plant operating and status information, including the cable length, termination status, and open fault and short fault locations. For more information about cable diagnostics with VeriPHY, see the *Programmers Guide for PHY Application Software* in the SparX-G5e collateral package.

Each copper PHY port also features four, direct-drive status LED pins per port. A serial LED mode is also available.

2.1.2 Tri-Speed Gigabit MACs

SparX-G5e implements 6 separate tri-speed Ethernet MACs, which comply with IEEE Std 802.3-2002. The tri-speed MACs provide support for full-duplex operation at 10/100/1000 Mbps and half-duplex operation at 10/100 Mbps. Five of the MACs connect to PHYs, and one of the MACs is connected directly to an exposed RGMII/GMII.

2.1.3 Quality of Service

SparX-G5e supports four QoS classes. On each port, an enhanced categorizer assigns priorities based on information taken from Layer 2 and Layer 3.

The categorizer analyzes all received frames. It assigns each frame to one of four QoS classes based on:

1. Port-based priority
2. User priority in the VLAN tag header (IEEE Std 802.1p)
3. Differentiated Services Code Point (DSCP) from the IP-header (IPv4 and IPv6 supported)

Based on the priority assigned by the categorizer, higher priority frames take precedence over lower priority frames during forwarding through the switching engine. In case of congestion, the lowest priority traffic is dropped before higher priority frames. In addition, the higher priority frames are able to overtake the lower priority frames in the queue, thereby minimizing latency for expedited data.

In this datasheet, the QoS class is also referred to as the internal frame priority.

2.1.4 Congestion Control

The ingress and egress directions on all ports can be configured to manage network congestion independently, either by dropping frames or by flow control pause frame signaling.

Flow control is guaranteed non-dropping for frame sizes up to about 4 kilobytes. Asymmetric flow control is supported for both the ingress and egress direction. Software can set up individual high and low thresholds for each FIFO. These thresholds control the starting and stopping of pause signaling. The internal FIFOs have enough memory to handle flow control on short-haul, full-duplex lines without using excessive pause signaling. The switch generates flow control pause frames, when necessary, to ensure that frames are never dropped.

In half-duplex mode, flow control is supported through back pressure.

In drop mode, SparX-G5e handles congestion situations by dropping frames intelligently according to bandwidth allocations, frame priorities, and available buffer capacity.

SparX-G5e features both strict priority-based forwarding and weighted-fairness forwarding, with guaranteed bandwidth allocation for the different QoS classes.

2.1.5 Frame Forwarding Analysis

The advanced filtering and forwarding capabilities in SparX-G5e are located in the analyzer module.

The analyzer maintains and uses four tables for frame forwarding: a source port table, a VLAN table, a MAC address table, and an aggregation mask table.

When the frame header information has been extracted from an incoming frame, the analyzer uses these tables to look up the following information:

- 8-bit source port mask.
- 8-bit VLAN mask.
- 8-bit destination port mask, if the DMAC address is known. If the DMAC address is not known, the analyzer looks up a programmable flooding mask.
- 8-bit aggregation port mask reflecting the selected port within a link aggregation group.

These four masks are then combined by a bit-by-bit AND operation and forwarded to the arbiter as the next forwarding decision for the given source port.

By default, the four masks are set up under the following conditions:

- Frames received on a given port cannot be forwarded to that same port.
- There is no VLAN present (all ports are members of all VLANs).
- Frames to a given destination address are forwarded only to the port where the destination was learned.
- There are no Link Aggregation Groups.

The job of the arbiter is to optimize the transfer of frames on the internal frame bus from the ingress queue system to the egress queue system. The arbiter decision is based on extensive information, such as frame priorities, port queue fillings, and egress shaper states.

2.1.6 MAC Address Learning

When a frame is received, the source MAC address is looked up in the MAC address table. For more information, see “Frame Forwarding Analysis,” page 32. If the address is not registered, and it is not a multicast address, a new entry is created. If necessary, an entry is discarded to make room for the new one based on a “least recently used” algorithm.

SparX-G5e is capable of looking up and adding all incoming entries to the MAC table at maximum load, which is known as “wire-speed learning”. Wire-speed learning reduces flooding in the network.

In addition, addresses can be learned and locked using an external CPU, or the internal CPU (V-Core CPU), by writing to the table. Locked entries are never discarded or aged.

2.1.7 VLAN Support

SparX-G5e can be configured as either VLAN unaware, behaving transparently toward VLAN-tagged frames, or as VLAN aware, where VLAN information is used in the forwarding decision. SparX-G5e can set up and maintain 4096 VLANs.

For a VLAN-aware switch, untagged frames are classified to a port specific, configurable VLAN identifier (VID). Frames that already have a VLAN tag when they are received are classified to the VID within the tag header in the frame.

VLAN-awareness (that is, tagging or untagging of frames) can be configured on a per-port basis. Each port can be configured to a set of ports to which it can forward, and thereby facilitate port-based VLANs. By default, all ports can forward to all other ports.

SparX-G5e supports both Independent and Shared VLAN Learning using Filter Identifiers (FID). An FID can be configured to a set of VIDs among which shared VLAN learning takes place. By default, independent VLAN learning is used.

2.1.8 Provider Bridging

SparX-G5e supports multiple VLAN tags, known as Q-in-Q, or VLAN stacking, which enables service providers to aggregate numerous independent customer LANs into the MAN space. With Q-in-Q tagging, the need for global VLAN coordination between the LANs is eliminated. Because each LAN and MAN has its own space of VLANs, there should be no shortage of VLAN identifiers.

SparX-G5e provides the following features:

- Each port can add or strip a VLAN tag (independently configurable for ingress and egress per port).
- Frame QoS class can be determined based on information in the outer VLAN tag.
- The frame can be forwarded, based on information in the outer VLAN tag.

The effective maximum frame size is 1526 bytes throughout the Q-in-Q network, because the standard end-station MTU of 1518 bytes may get two VLAN tags each, with 4 bytes inserted.

2.1.9 DSCP Remarking

SparX-G5e supports DSCP remarking, where the DSCP value in IPv4 or IPv6 packets is remarked to a new value based on the assigned frame QoS class. DSCP remarking is a key feature in making edge network equipment assign a QoS class that can be used throughout the network. DSCP remarking, combined with proper QoS settings, is a basic requirement to support quality VoIP applications reliably.

2.1.10 IP Multicast

SparX-G5e provides enhanced support for IP Multicast by allowing up to 8,192 programmable multicast groups to co-exist in the MAC table. This, in combination with IGMP snooping where IPMC membership information is passed on to the CPU, enables applications such as digital video distribution.

2.1.11 Flooding Storm Control

SparX-G5e features a flooding control system for constraining undesired behavior caused by, for example, loops in the network or denial-of-service attacks.

2.1.12 Link Aggregation

SparX-G5e supports ingress and egress port aggregation in accordance with IEEE Std 802.3ad. Any number of ports can be aggregated into any number of groups. Frames are distributed among the aggregated ports by an advanced frame distribution function, which, through configuration, can use the following information:

- Source and destination MAC addresses
- Source and destination IP addresses
- TCP/UDP port numbers for IPv4 packets
- Flow label for IPv6 packet
- Pseudo-randomization

2.1.13 CPU Interfaces and V-Core CPU

SparX-G5e provides three interfaces to core registers:

- An 8-bit parallel interface (PI)
- An on-chip 8051 CPU interface
- A serial, SPI-style, four-wire interface (SI)

The serial interface exists in all configurations of SparX-G5e. It allows interfacing to many different types of microcontrollers and is capable of transferring approximately 20 Mbps.

The parallel interface and the on-chip 8051 CPU (V-Core CPU) interface are mutually exclusive, because they use the same external interface. The selection between the two is made with a strapping pin ICPU_PI_En. Strapping the pin low enables the parallel interface, whereas strapping it high enables the V-Core CPU.

- With the ICPU_PI_En pin strapped low, SparX-G5e operates as a slave on an external CPU's parallel bus. The V-Core CPU is still operable, but needs to be boot strapped either by an external CPU or through a serial PROM attached to the serial interface.The PI interface can be configured to run in 8-bit mode, allowing it to work with an 8-bit CPU system, such as an external 8051 controller.

  The parallel interface can manage up to about 160 Mbps. This corresponds, approximately, to a maximum receive frame rate of 278 kiloframes per second for 64-byte frames and 13 kiloframes per second for 1518-byte frames. The maximum transmit frame rate is approximately 199 kiloframes per second for 64-byte frames and 12 kiloframes per second for 1518-byte frames. The listed frame rates include required overhead, such as reading and writing the Internal Frame Header and checking for buffer overflow.
- With the ICPU_PI_En pin strapped high, the V-Core CPU boots from the previously mentioned parallel interface, which is now used as a RAM/Flash interface and is therefore not usable by external microcontrollers.The V-Core CPU is a standard 8-bit 8051 microcontroller with a number of add-on modules extending the basic 8051 functionality. It is designed to replace the functionality of an externally attached CPU, such as switch monitoring and configuration, frame capture and transmission for STP and GxRP (GARP, GVRP, GMRP) protocols, as well as direct access to the output queues.

In addition to standard 8051 functionality, the V-Core CPU features 8 kilobytes of on-chip RAM, which is accessible as both program and data memory, and 256 bytes of scratchpad RAM (internal RAM). Both RAMs can be accessed from an external CPU connected to the SI interface (independent of ICPU_PI_En) or PI interface (ICPU_PI_En strapped low).

The glueless connection to most commercial flash memories (Flashes) and RAMs is made through the shared 16-bit address and 8-bit data buses, with the option to extend the address bus with four bits through a paging mechanism, which allows up to 1 megabyte of external data RAM and up to 1 megabyte of external program memory (Flash or ROM). The external interface's read and write timing can be configured separately for read and write accesses and for code and data accesses.

The V-Core CPU uses only 4 clock cycles per instruction compared to the original 8051 CPU, which uses 12 clock cycles. In addition, the clock frequency can be changed dynamically (4.88 MHz – 78.125 MHz) to meet the timing of external memories and to speed up execution if running in internal memories only.

The V-Core CPU has access to a standard RS232 interface, three timers, a watchdog, and two additional GPIO pins, one of which may be used for externally controlled program single-stepping. Another application of the GPIO pins is to use them in a pair as a two-wire serial interface for connecting to SFP modules.

Software synchronization and handshaking between the V-Core CPU and an optional external CPU connected to the SI interface of the SparX-G5e device is possible using a mailbox accessible by both CPUs.

The V-Core CPU supports industry-standard compilers and assemblers.

An external EEPROM can initiate booting of the V-Core CPU through the SI interface. This feature is enabled when ICPU_PI_En and ICPU_SI_Boot_En are both strapped high.

2.1.14 Register Access

The register control block receives commands from either the V-Core CPU or from an off-chip controller/processor. The commands can be divided into four categories:

- MII Management reads and writes for PHY control
- Configuration
- Status or statistics gathering
- Capturing and transmitting frames

2.1.15 MII Management Interface

SparX-G5e has two built-in MII Management controllers for setting up and monitoring status of the internal PHYs and the externally connected PHYs. Controller 0 is connected to the internal PHYs; controller 1 is suitable for direct connection to standard RGMII/GMII PHYs.

2.1.16 General-Purpose I/Os

SparX-G5e features four general-purpose I/O pins (GPIO). The pins are freely configurable as either inputs or outputs, and are accessed through either of the CPU interfaces.

In addition to the device's four GPIO pins, VSC7395 features four, direct-drive LED status pins per port, with the option of using any of these as general purpose outputs by using the “force mode” feature of these pins. For more information about force mode, see “Parallel LED Output,” page 55. When used in combination, these flexible GPIOs and LED pins can be used, for example, to control external SFPs, to interface with Power-over-Ethernet (IEEE Std 802.3af) controllers, or to signal VeriPHY cable diagnostic status events with external LEDs.

2.1.17 Counter Support

SparX-G5e has a configurable set of counters for gathering statistics. Each port has an Rx and a Tx byte counter, as well as three Rx and three Tx frame counters. The Rx and Tx frame counters are configurable to count any event in the RMON groups 1, 2, 3, and 9.

2.1.18 Royalty-Free Web-Managed Software Stack with SNMP

Vitesse provides a royalty-free software stack for web-managed systems for the SparX-G5e device. This software stack enables quick and easy development of a comprehensive web-managed solution that runs on the on-chip 8051 CPU. The software stack includes a TCP/IP stack, a web server with reference web pages, and an SNMP server with reference MIBs. Full source code for the KEIL C compiler is provided. For more information, see the *RBM0007 Software Manual*.

3 Functional Descriptions

The different aspects of the SparX-G5e switching engine are explained in detail in the following section. References are often made to the register set. For more information about the various registers, see "Device Register Details," page 150 and following pages.

Additional optional features and settings are available. For more information about these features and settings, see "Registers," page 129.

3.1 Port Numbering

Five front ports on SparX-G5e are attached to five PHYs, which, in turn, are attached to five MACs. One port is directly attached to a MAC enabling the exposed RGMII/GMII. The mapping from front port to PHY to MAC is listed in the following table.

Table 1. Port Numbering for PHYs and External RGMII/GMII

Front Port	PHY	MAC
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
RGMII/GMII port		6

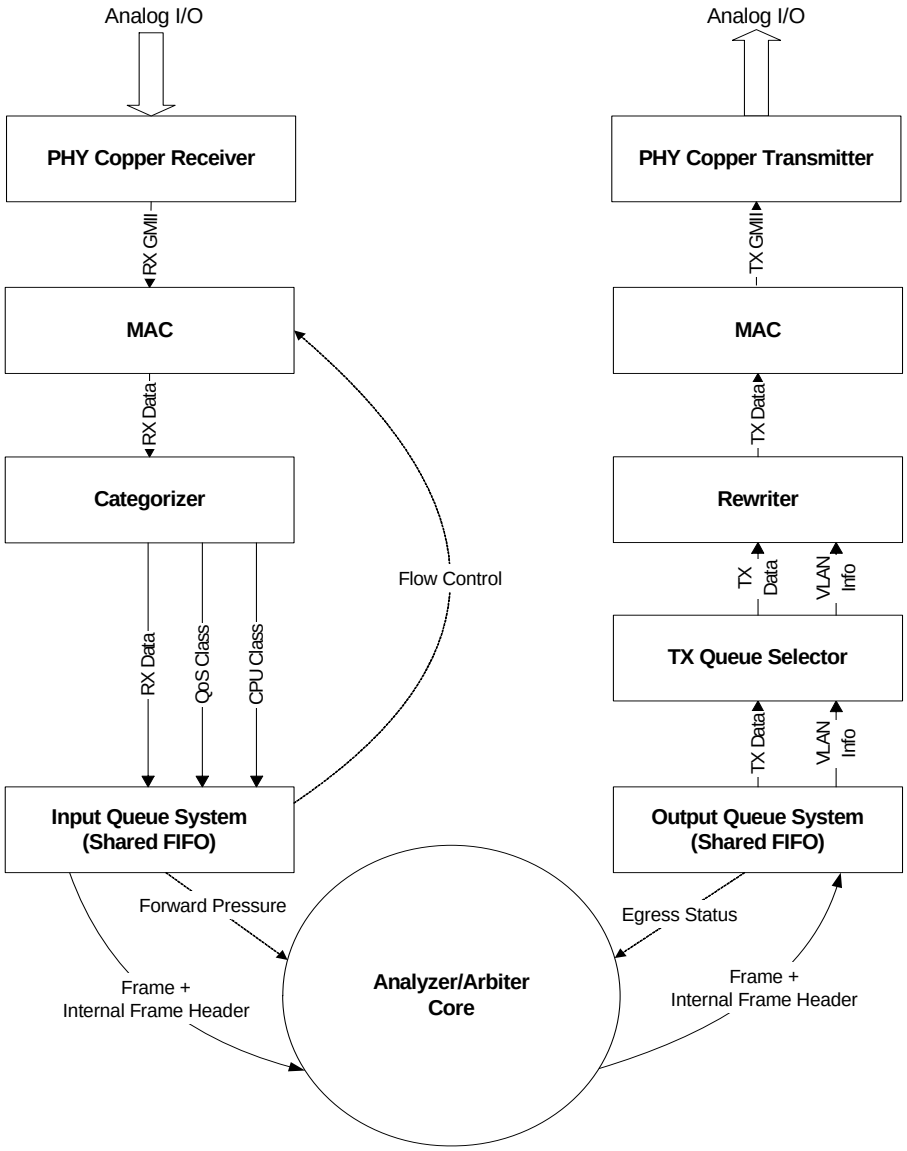
Note that when monitoring or configuring port specific registers for the RGMII/GMII port, MAC 6 must be accessed. Bit positions in port masks, used extensively when configuring the SparX-G5e device, correspond to the MAC numbers. Thus, the RGMII/GMII port is bit 6 in a mask.

In the following, and in particular in the register descriptions in "Device Register Details," page 150, the term "port" relates to the MAC in the switch engine and *not* the front port of the SparX-G5e device. Where necessary, the term "front port" is used to differentiate the actual front port of SparX-G5e from a MAC.

3.2 Introduction – A Frame's Life In SparX-G5e

For the following topics, several blocks of SparX-G5e shown in Figure 1 are explained by looking at a frame's life in the SparX-G5e device. The following figure illustrates how the blocks interact as a frame passes through them.

Figure 2. The Life of a Frame



3.3 Switch Engine Operation and Congestion Control

This section describes the use of priorities in the forwarding scheme. A port can operate in either drop mode, where frames are dropped if resources are depleted, or in flow control mode, where incoming traffic is paused when resources are depleted. The following information describes drop mode. For more information about the mechanisms involved when running flow control mode, see "Flow Control Mode," page 44.

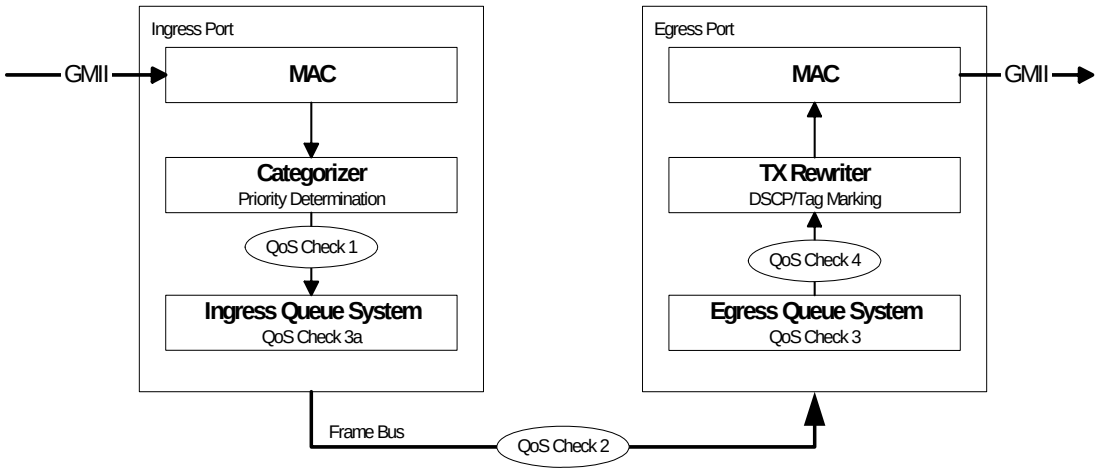
3.3.1 Quality of Service Scheme

The queue system and forwarding mechanisms in the SparX-G5e device are based on a priority property assigned to each frame received from the front ports. In the ingress path, the categorizer examines the frame data and assigns a priority in the range of 0 to 3. This property is used when evaluating which frames to forward first in the switch core, and which frames to drop when memory resources get depleted. Higher priority values are evaluated as being of higher importance.

The priority is monitored several times during the frame forwarding process. The following steps correspond to the QoS Check numbers shown in Figure 3.

1. When frames are enqueued into the ingress queue system, the priority determines limits for memory filling. When the limit is reached, the frame is dropped.
2. When frames are to be forwarded to the egress queue systems through the internal frame bus, the highest priority frames are sent before others.
3. When frames are forwarded to egress queue systems, the priority determines limits for egress memory filling. When the limit is reached, the frame can be dropped.
4. When frames are dequeued from the egress queue systems, the Tx Queue Selector determines which queue should forward the frame.

Figure 3. QoS Overview



3.3.2 Queue System Memory

Each port contains an ingress queue system and an egress queue system. Each system contains four queues, one for each priority. The egress queue system also contains a CPU transmit queue, which is always emptied before others.

Table 2. Queues per Port

Queue	Frames Stored
Ingress Queue 0	Ingress frames with QoS class 0
Ingress Queue 1	Ingress frames with QoS class 1
Ingress Queue 2	Ingress frames with QoS class 2
Ingress Queue 3	Ingress frames with QoS class 3
Egress Queue 0	Egress frames with QoS class 0
Egress Queue 1	Egress frames with QoS class 1
Egress Queue 2	Egress frames with QoS class 2
Egress Queue 3	Egress frames with QoS class 3
Egress CPU Transmit Queue	Egress frames written through the CPU interface

The queues are all stored in the memory pool for the port, which is 20 kilobytes. The memory pool is shared between the ingress and egress queues. Using watermarks, it can be freely chosen how much to use for each of the traffic directions. When frames are inserted into a queue, watermarks configured for the priority of the frame are used for evaluating drop conditions for the frame. These watermarks are all found in the Q_DROP_WM/Q_FLOWC_WM registers with MIN and MAX watermarks per priority 0-3. The unit for all watermarks is 512 bytes.

To enable the 20-kilobyte memory pool, Q_MISC_CONF::EXTENT_MEM must be set to 1 before releasing the port from reset. Otherwise, a 16-kilobyte memory pool is used.

Table 3. Watermarks per Port

Watermarks	Compared With
INGRESS_MIN(QoS class)	The size of the ingress queue for incoming frame
INGRESS_MAX(QoS class)	The amount of data in all ingress queues
EGRESS_MIN(QoS class)	The size of the egress queue for forwarded frame
EGRESS_MAX(QoS class)	The amount of data in all egress queues
FWDP	The amount of data in all ingress queues

For more information about watermark configuration, see “Suggested Watermark Settings,” page 44.

3.3.3 Ingress Enqueueing

When a frame is to be enqueued into the ingress queue system on the ingress port, some QoS evaluations take place to drop frames of lower class before higher.

QoS Check 1: Frame of QoS class <Qos class> about to get enqueued
Drop frame when: - Both INGRESS_MIN(QoS class) and INGRESS_MAX(QoS class) are reached. Otherwise the frame is added to the QoS class selected queue.

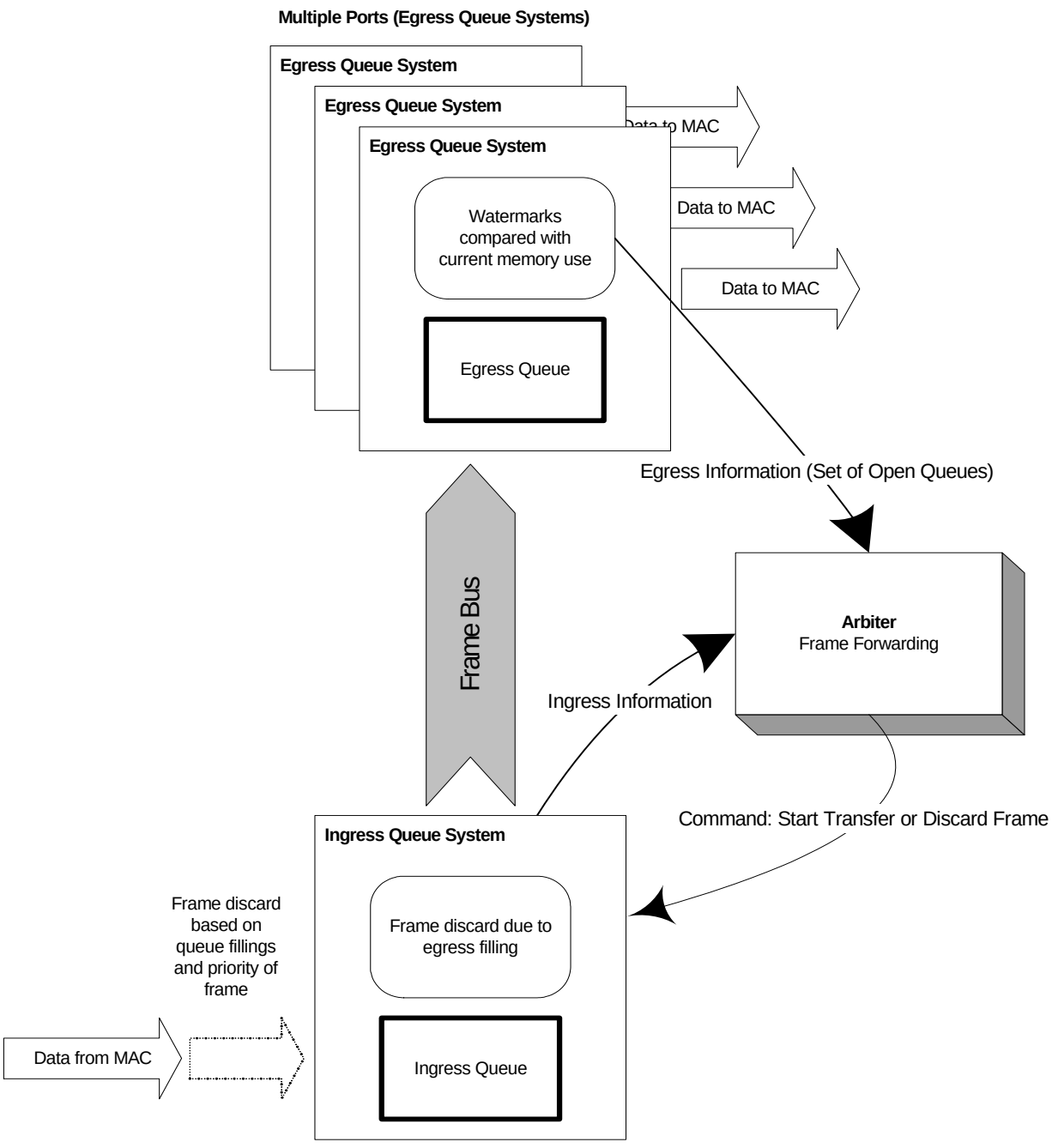
For example, the amount of lowest priority traffic can be limited to 1.5 kilobytes by setting INGRESS_MIN(0) to 3.

3.3.4 Internal Frame Forwarding

Figure 4 shows the overall frame forwarding mechanisms in SparX-G5e and should be used for general reference when reading the following.

Frames from the ingress queue systems are transferred to the egress queue systems according to commands from the central arbiter. Higher priority always takes precedence over lower priority. Equal priorities are serviced in a round robin fashion when multiple ingress queue systems with equal priorities have frames pending for the same egress queue system. This principle is shown as QoS check 2 in the following figure.

Figure 4. Frame Forwarding



The goal of the central arbiter is to forward frames between ingress and egress queue systems, avoiding the forwarding of data that is dropped due to lack of storage capabilities at the destination. Some Egress queue systems may be overloaded with data, and therefore, not able to enqueue more frames. This is the case, for example, when an ingress system attached to a MAC running 1 Gbps is forwarding data to an egress system attached to a MAC running 100 Mbps.

This problem is handled in the arbiter through inspecting queue fillings in all egress queue systems, and taking this into account when optimizing frame transfers. Briefly, frames that are to be forwarded to overfilled egress queues are either suspended or dropped from the ingress queue system immediately.

QoS Check 3: Frame of QoS class <QoS class> to be forwarded to egress system
Egress system cannot accept frame when: - Both EGRESS_MIN(QoS class) and EGRESS_MAX(QoS class) are reached. Otherwise, the egress queue system allows the arbiter to forward frame data.

When the above check is holding back frames in the ingress queues, QoS check 3a is activated. This check guarantees that frames are discarded when there is no more room in the destination egress systems, and the ingress system is starting to get depleted.

QoS Check 3a: Frame of QoS class <QoS class> cannot be forwarded due to check 3
Frame is discarded when: - The FWDP watermark is reached. Otherwise, the frame forwarding or dropping is suspended until changes occur to the fillings.

3.3.5 Egress Dequeuing and Transmission

The egress queue system features a Tx Queue Selector that provides a way of guaranteeing bandwidth allocation for the different QoS classes (QoS check 4). This is required when using weighted priority, where egress bandwidth is shared among the available QoS classes.

The Tx Queue Selector is configured per port through the TXQ_SELECT_CFG register. By default, the egress queue system is set up for strict priority, where higher QoS classes always are transmitted before lower classes. Weighted priority is enabled through TXQ_SELECT_CFG::WEIGHTED_PRIO_ENA. When enabled, the Tx Queue Selector selects the next queue for transmission by cycling through 10 configurable slots indicating which one of the four queues the next frame is taken from. Thus, the 10 slots provide a 10% granularity for the egress rates per QoS class, making it possible, for example, to assign 40%, 40%, 10%, and 10% of the egress rate to the four QoS classes.

The Tx Queue Selector is not an egress bandwidth limiter, because excess bandwidth is always given to queues with frames ready for transmission in a strict priority fashion.

If a QoS class is not listed in the 10 slots, frames with that QoS class are only transmitted when excess bandwidth is available.

Frames transmitted through the CPU always take highest priority and, as a result, are transmitted as quickly as possible.

It is possible to disable 2 of the 10 slots through TXQ_SELECT_CFG::REDUCED_ENA. This is convenient, for example, when all four QoS class must have equal rates (25%).

3.3.6 Flow Control Mode

When the switch is configured for flow control mode, frame drops are not accepted, and therefore, the ingress drop commands issued from the arbiter (see Figure 4) are not allowed. This can be disabled through the SBACKWDROP and DBACKWDROP register in the frame arbiter register block. In this mode, the FWDP watermark is instead used for asking the ingress MAC to issue pause frames, thereby protecting the ingress queue system from overflow. The FWDP watermark operates with hysteresis, and is thus configured with a start and a stop value. For more information about the FWDP watermark, see the Q_FLOWC_WM register in Table 108, page 167.

In general, flow control mode requires the ingress and egress watermarks in Q_DROP_WM and Q_FLOWC_WM to be set up carefully to ensure non-dropping performance. For more information about specific setup rules, see "Flow Control Setup," page 45.

Asymmetric flow control is also supported, because ingress and egress flow control can be enabled separately. Egress flow control, where incoming pause frames are obeyed and the egress traffic is paused, is enabled or disabled in FCCONF::FLOW_CTRL_OBEY. Ingress flow control, where ingress congestion situations are handled by issuing pause frames to halt the link partner, is enabled or disabled in Q_FLOWC_WM::MAC_PAUSE_MODE.

3.3.7 Suggested Watermark Settings

The setting of the various watermarks has a major influence on how frames from different priorities are handled in oversubscribed scenarios, where some of the traffic must be dropped. In general, the QoS behavior is described as running with strict priority or with weighted priority.

Strict QoS means always letting higher priority frames be handled before others; if lack of resources arises, always drop the lowest prioritized frames. Weighted QoS means sharing the resources between the possible priorities, in terms of a guaranteed amount of the memory pool, and a guaranteed amount of the egress bandwidth.

Note The watermarks in these examples are only used to clarify the use of the watermarks. The settings are not optimal, as the term "optimal" is strongly dependent on the properties of the traffic in the network.

3.3.7.1 Strict Priority Setup

If a port is oversubscribed, and the highest priority is configured to use all memory, all the INGRESS_MIN(QoS class) or EGRESS_MIN(QoS class) watermarks must be zero, and the INGRESS_MAX(QoS class) or EGRESS_MAX(QoS class) watermarks must be configured with increasing priority value.

An example of this setup is shown in the following table.

Table 4. Strict Priority Setup Example

QoS Class Watermarks	Value (Slices of 512 Bytes)
INGRESS_MIN(0-3)	0,0,0,0
INGRESS_MAX(0-3)	12,14,16,18
EGRESS_MIN(0-3)	0,0,0,0
EGRESS_MAX(0-3)	12,14,16,18
FWDP	6

3.3.7.2 Weighted Priority Setup

If a port is oversubscribed, and memory is to be shared between all priorities, all the watermarks must be nonzero. An example of this setup is shown in the following table.

Table 5. Weighted Priority Setup Example

QoS Class Watermarks	Value (Slices of 512 Bytes)
INGRESS_MIN(0-3)	4,4,4,4
INGRESS_MAX(0-3)	11,11,11,11
EGRESS_MIN(0-3)	4,4,4,4
EGRESS_MAX(0-3)	11,11,11,11
FWDP	6

3.3.7.3 Flow Control Setup

Flow control and QoS principles hardly co-exist, as the flow control mechanisms according to IEEE Std 802.3 are unaware of traffic priorities. In flow control mode, the rule is: do not drop any frames at all. If, for example, the lowest prioritized traffic is oversubscribing the egress port for which it is destined, all of the incoming frames must be paused. An example of this configuration is shown below.

Thresholds must be set with care to avoid frame loss in all cases (provided that no pause frames are lost). The amount of data that can possibly be received from the moment the MAC is asked to send a pause frame until the last byte from the remote partner has been received is:

2 × (maximum frame size) +	[media occupied]
2 × (cable length) × 5 bits × (speed / 1000) +	[data on cable]
250 bytes	[various reaction times]

This value varies for different speeds and cable lengths, as shown in the following table. Standard Ethernet frame sizes are assumed with sizes up to 1526 bytes (double-tagged standard-sized frames).

Table 6. Flow Control Data Receivable After Pause Frame

Speed (Mbps)	Length			
	10 m	100 m	550 m	2000 m
10	3.1 kilobytes	3.1 kilobytes		
100	3.1 kilobytes	3.1 kilobytes		
1000	3.1 kilobytes	3.2 kilobytes	3.8 kilobytes	5.8 kilobytes

When setting the thresholds, it is beneficial to have as large a part of the pool memory allocated for egress data as possible. This can be done by setting the thresholds using the values from Table 6 in place of the "X" in Table 7.

Table 7. General Flow Control Settings to Avoid Frame Loss

Threshold	Value
FWDP_START	4 kilobytes (at least two max size frames)
FWDP_STOP	3.5 kilobytes (a small hysteresis)
INGRESS_MIN(0-3)	0
INGRESS_MAX(0-3)	FWDP_START + X from Table 6
EGRESS_MIN(0-3)	0
EGRESS_MAX(0-3)	20 kilobytes – INGRESS_MAX

As an example, the configuration for a 1-Gbps port on a 550-meter media results in the thresholds shown in the following table.

Table 8. 1-Gbps Port Configuration Example

Threshold	Value (Slices of 512 Bytes)
FWDP_START	12
FWDP_STOP	11
INGRESS_MIN(0-3)	0
INGRESS_MAX(0-3)	20
EGRESS_MIN(0-3)	0
EGRESS_MAX(0-3)	20

Apart from the watermark settings, SBACKWDROP and DBACKWDROP must be set to zero.

3.3.8 Advanced Forwarding Options

3.3.8.1 Round Robin Exceptions

To ensure fair bandwidth allocation between ingress ports, the arbiter can be configured to allow repeated forwarding from the same ingress system, even when multiple ingress ports have frames ready for the same destination. This is done through the ARBBURSTPROB register found in the Frame Arbiter register block. This register allows you to set each port to send multiple frames in a row with a certain probability. It is recommended to set a small value of 1-2 in this register, which, in special scenarios, provides better bandwidth sharing between ingress ports.

3.3.8.2 Forced Discard of Frames from Specific Ingress Ports

When a port must be reset, the ingress queues for that port must be emptied before beginning the reset process. This is done using the ARBDISC register in the arbiter block; for more information, see Table 140, page 177.

3.3.9 Jumbo Frames

SparX-G5e supports jumbo frames of up to 9.6 kilobytes. The default configuration of the SparX-G5e device is set to a maximum length of 1518 bytes, but this can be changed through the MAXLEN and PHY_CTRL_EXT2 registers. A jumbo frame is any frame larger than the maximum standard-sized frame of 1526 bytes (double-tagged 1518-byte frame).

Jumbo frames are supported at all three speeds (10/100/1000 Mbps).

Because the shared pool for frames in each port is limited to 20 kilobytes, the thresholds must be carefully chosen to allow flows of relatively large frames. Otherwise, the pool control system drops frames before they are fully stored. This is handled through the watermark registers Q_DROP_WM and Q_FLOWC_WM. In jumbo mode, frame loss must be expected in fully meshed traffic scenarios. However, in Gigabit mode, non-dropping bi-directional throughput is supported up to 9.6-kilobyte frames.

Jumbo frame performance is significantly affected by a number of factors, such as watermark settings or test configuration type (including point-to-point or fully meshed, unidirectional or bidirectional traffic, maximum packet length). For more information, contact your Vitesse Field Applications Engineer.

3.3.9.1 Early Transmission

For ports running at 1 Gbps, a feature called Early Transmission is available to improve forwarding of large jumbo frames. The feature is similar to a cut-through mode, allowing an egress MAC to initiate transmission of a frame before the transfer of the frame on the frame bus from ingress to egress is complete. The obvious advantage is that less buffer is needed for storage in the egress port, because the buffer is being emptied at the same time as it is being filled. Early Transmission is enabled and configured in Q_MISC_CONF::EARLY_TX.

3.3.9.2 QoS and Jumbo Frames

The size of the memory available for storing frames limits the performance of jumbo frames of multiple priorities at the same time. Either all frames should be classified for equal priority, or only frames with the highest priority can be allowed to have jumbo size (by setting the lower priority thresholds much lower than the highest). For smaller sizes of jumbo frames, such as 6 kilobytes, some degree of QoS may be possible.

3.3.9.3 Flow Control and Jumbo Frames

The use of flow control on ports with jumbo frames has limitations. This is because the amount of excess data that can arrive between the time a pause frame is required to be transmitted and the time at which the remote partner stops transferring more data can be as much as two maximum sized frames.

The sequence in flow control is:

1. The MAC starts transmission of a maximum size frame.
2. Shortly afterward, the thresholds trigger a pause frame transmission.
3. The MAC finalizes transmission from step 1 and initiates the pause frame (step 2).
4. The remote link partner initiates a maximum size frame transmission.
5. Shortly afterward, the remote partner receives the pause frame initiated in step 3.
6. The remote partner finalizes the maximum size frame transmission begun in step 4.
7. The remote partner suspends transmission due.

The delay from step 2 to step 7 is more than two maximum-sized frames, which in the case of jumbo frames is a large amount of available memory. (For more information, see "Flow Control Setup," page 45.) As a rule, non-dropping, non-excessive flow control is possible up to 3-kilobyte jumbo frames.

3.4 PHY Functionality and Setup

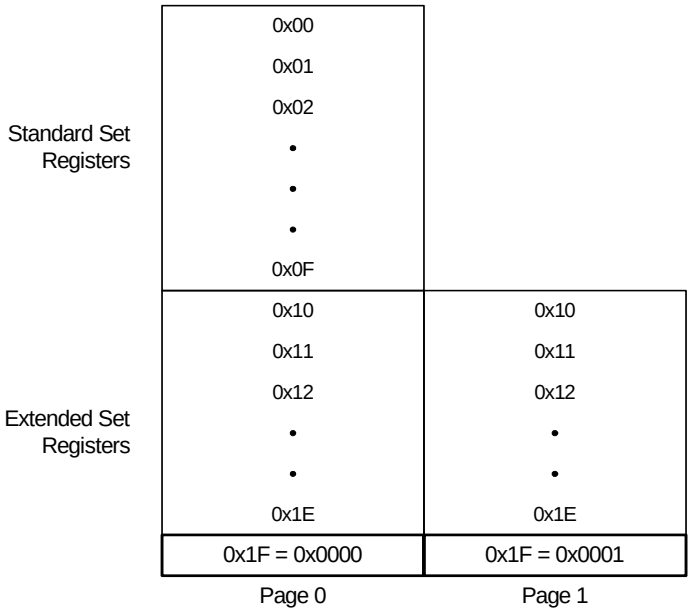
This section describes the high level setup and operation of the built-in PHYs of SparX-G5e. The integration of the PHYs is kept as close to multi-chip PHY/Switch hardware designs as possible. This allows a fast migration path for software already running in a similar distributed design while still benefitting from the cost savings provided by the SparX-G5e integration.

3.4.1 Register Access

The registers of the PHYs are not placed in the memory map of the Switch and the MAC, but are attached instead to the built-in MII management controller 0 of SparX-G5e. Therefore, PHY registers are accessed indirectly through the Switch registers. For more information, see "MII Management Bus," page 89.

Apart from providing the IEEE Std 802.3 specified 16 MII Standard Set registers, the PHYs contain an Extended Set of registers that provide additional functionality. Different memory pages are accessed by changing the view of the upper half of the memory map. This is controlled through PHY_MEMORY_PAGE_ACCESS::PAGE_ACCESS_CFG. The memory layout of the PHYs is illustrated in the following figure.

Figure 5. PHY Memory Layout



3.4.1.1 Broadcast Write

The PHYs can be configured to accept MII PHY register write operations, regardless of the destination address of these writes. This is enabled in PHY_CTRL_STAT_EXT::BROADCAST_WRITE_ENA. This enabling allows similar configurations to be sent quickly to multiple PHYs without having to do repeated MII PHY write operations. This feature applies only to writes; MII PHY register read operations are still interpreted with "correct" address.

3.4.1.2 Reset of Registers

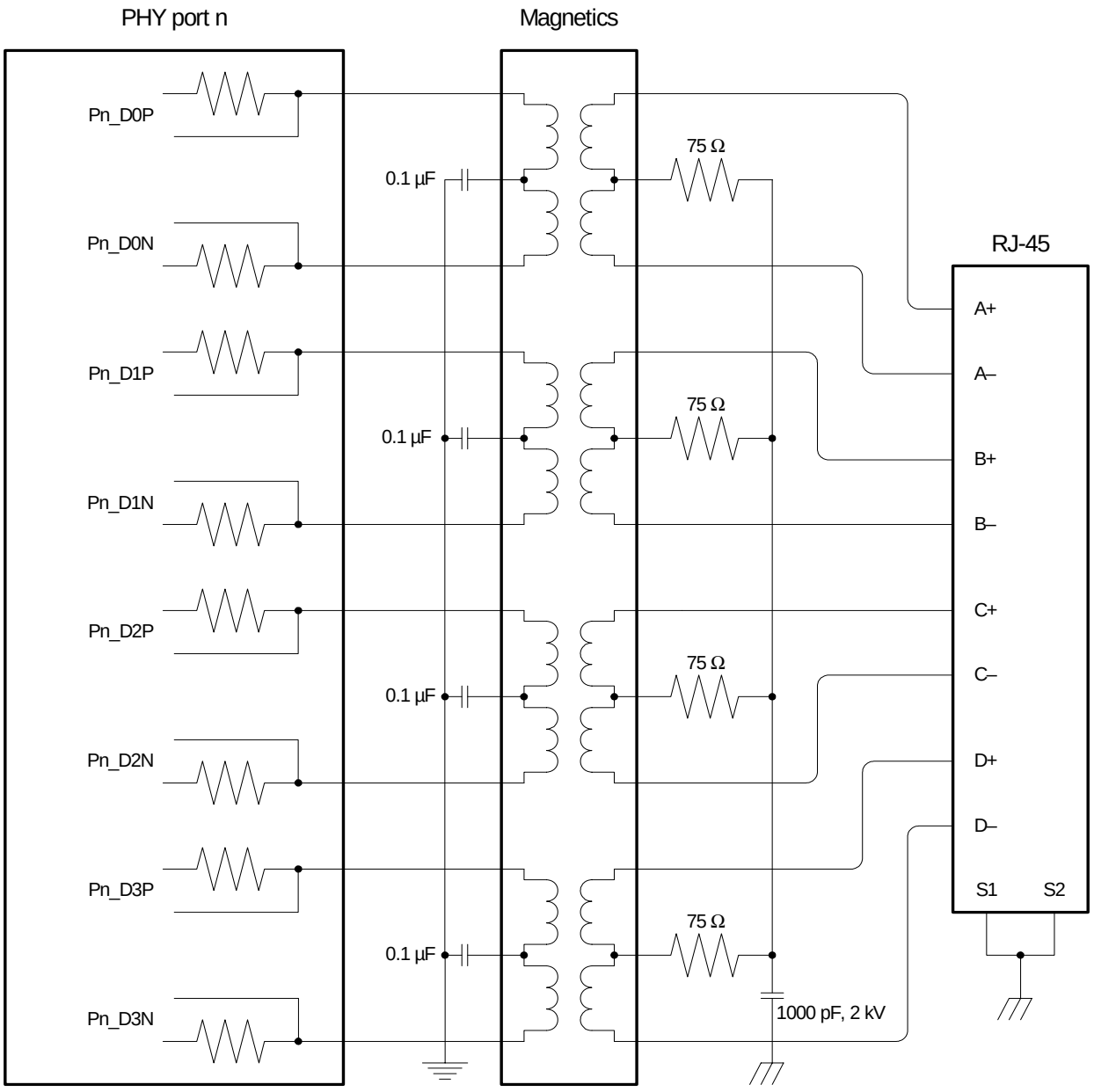
The PHY can be reset through software. This is enabled in PHY_CTRL::SOFTWARE_RESET_ENA. Enabling this field initiates a software reset of the PHY. Fields that are *not* described as sticky are returned to their default values. Fields that are described as sticky are only returned to defaults if sticky-reset is disabled through PHY_CTRL_STAT_EXT::STICKY_RESET_ENA. Otherwise, they retain their values from prior to the software reset. A hardware reset always brings all PHY registers back to their default values.

After a reset of the PHY, rerun the PHY initialization sequence. For more information about the PHY initialization sequence, see "Initialization Sequence," page 140.

3.4.2 Twisted Pair Interface

The twisted pair interface on SparX-G5e is fully compliant with the IEEE Std 802.3-2002 specification for Category-5 (Cat5) media. The SparX-G5e PHY, unlike other traditional gigabit PHYs, integrates all of the line termination resistors (required to connect the PHY's Cat5 interface to an external 1:1 transformer) into the device. This reduces the number of components in a system design and greatly simplifies the layout of this interface. The connection of the twisted pair interface is shown in the following figure.

Figure 6. Twisted Pair Interface



Unlike gigabit PHYs which do not integrate the line terminations into the PHY, the VSC7395 PHYs' twisted-pair interface is compatible with a wide variety of standard magnetics and RJ-45 modules from common module vendors.

Depending on the application (for example, the number of ports, EMI performance requirements such as FCC Class A or B, the quality and type of the equipment shielding, and overall approach to EMI design practice), the twisted-pair interface is designed to be compatible with standard magnetics modules from a wide variety of vendors.

For more information, see the *SparX Magnetic Selection and EMI Control* application note at the Vitesse Web site at www.vitesse.com.

3.4.2.1 Auto-Negotiation

SparX-G5e supports twisted pair auto-negotiation, as defined in IEEE Std 802.3-2002 clause 28. This process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, auto-negotiation can determine speed, duplex, and master/slave modes for 1000BASE-T. Auto-negotiation also allows SparX-G5e to communicate with the link partner (through optional Next-Pages) to set attributes that may not be defined in the standard.

If the link partner does not support auto-negotiation, SparX-G5e automatically uses parallel-detect to select the appropriate link speed. Clause 28 twisted-pair auto-negotiation can be disabled in PHY_CTRL::AUTONEG_ENA. If auto-negotiation is disabled, the operating speed and duplex mode of SparX-G5e is determined by the state of the fields SPEED_SEL_MSB_CFG, SPEED_SEL_LSB_CFG, and DUPLEX_MODE_CFG in the PHY_CTRL register.

Auto-negotiation can be restarted by writing to PHY_CTRL::AUTO_NEG_RESTART_ENA. This field is automatically cleared after auto-negotiation is restarted. The status of the auto-negotiation process can be monitored in PHY_STAT::AUTONEG_COMPLETE. Errors that occur during parallel-detect are reported in PHY_AUTONEG_EXP::PARALLEL_DET_FAULT.

PHY_STAT_1000BT::MS_CFG_FAULT stores the results of the auto-negotiated master/slave timing in 1000BASE-T. If errors occur in the process of auto-negotiating master/slave timing, they are reported through the PHY_STAT_1000BT::MS_CFG_RESOLUTION.

3.4.2.2 Auto MDI/MDI-X Function

For trouble-free configuration and management of Ethernet links, SparX-G5e includes robust Automatic Crossover Detection functionality for all three speeds on the twisted pair interface (10BASE-T, 100BASE-TX, and 1000BASE-T) — fully compliant with the IEEE standard.

In addition to the IEEE standard, SparX-G5e detects and corrects polarity errors on all MDI pairs.

Automatic MDI/MDI-X can be disabled in PHY_BYPASS_CTRL::PAIR_SWAP_DIS. The status of this function is located in PHY_AUX_STAT_CTRL::MDI_MDX_X_IND and PHY_AUX_STAT_CTRL::CD_PAIR_SWAP.

Automatic Polarity Correction can be disabled in PHY_BYPASS_CTRL::POL_INV_DIS. Status information for this function is found in the fields A_POL_INVERSION, B_POL_INVERSION, C_POL_INVERSION, and D_POL_INVERSION in the PHY_AUX_STAT_CTRL register.

SparX-G5e's Automatic MDI/MDI-X algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 9. Accepted MDI Pair Connection Combinations

RJ-45 Connections				
1,2	3,6	4,5	7,8	Comments
A	B	C	D	Normal MDI mode
B	A	D	C	Normal MDI-X mode
A	B	D	C	MDI mode Pair swap on C and D pairs
B	A	C	D	MDI-X mode Pair swap on C and D pairs

Auto MDI/MDI-X in Forced 10/100 Link Speeds

SparX-G5e includes the ability to perform Auto MDI/MDI-X, even when auto-negotiation is disabled and the link is forced into 10BASE-T and 100BASE-TX link speeds. (For more information about auto-negotiation, see "Auto-Negotiation," page 51.) To enable this feature, additional PHY MII register write settings are needed in the following order:

To enable Auto MDI/MDI-X in forced 10/100 link speeds:

1. Write 0x52B5 to PHY MII Register 0x1F.
2. Write 0x0012 to PHY MII Register 0x12.
3. Write 0x3803 to PHY MII Register 0x11.
4. Write 0x87FA to PHY MII Register 0x10.
5. Write 0x0000 to PHY MII Register 0x1F.
6. Write 0 to PHY MII Register 0x12, bit 6.

To disable Auto MDI/MDI-X in forced 10/100 link speeds:

1. Write 0x52B5 to PHY MII Register 0x1F.
2. Write 0x0012 to PHY MII Register 0x12.
3. Write 0x2003 to PHY MII Register 0x11.
4. Write 0x87FA to PHY MII Register 0x10.
5. Write 0x0000 to PHY MII Register 0x1F.
6. Write 1 to PHY MII Register 0x12, bit 6.

3.4.2.3 Twisted Pair Link Speed Downshift

In addition to automatic crossover detection, SparX-G5e supports an automatic link speed "downshift" option for operation in cabling environments that are incompatible with 1000BASE-T. This feature can be enabled in PHY_CTRL_EXT3::SPEED_DOWNSHIFT_ENA.

When enabled, SparX-G5e automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. This is especially useful in setting up networks using older cable installations that may include only pairs A and B and not pairs C and D. The number of failed auto-negotiation advertisement attempts is configured in PHY_CTRL_EXT3::SPEED_DOWNSHIFT_CFG. The status of this function can be monitored through PHY_CTRL_EXT3::SPEED_DOWNSHIFT_STAT.

3.4.2.4 Transformerless Ethernet Operation

The twisted pair interface supports 10/100/1000BASE-T Ethernet for IP-based backplane applications, such as those specified by the PICMG™ 2.16 and ATCA™ 3.0 specifications for 8-pin channels. With proper AC coupling, the typical Cat5 transformer (magnetics) can be removed and replaced with capacitors.

Enabling the PICMG reduced power mode can reduce power consumption to less than 600 mW per port. This is enabled in PHY_CTRL_EXT2::PICMG_REDUCED_POWER_ENA.

3.4.3 Gathering Status Information

The PHY has a number of register fields that can be used for collecting status information from the PHY:

- Link, Speed, and Duplex Indications
- General Fault Indications
- 10BASE-T Indications
- 100BASE-TX Indications
- 1000BASE-T Indications

3.4.3.1 Link, Speed, and Duplex Indications

The Cat5 media link status is indicated in PHY_STAT::LINK_STAT. This field shows whether the PHY has a link on the twisted pair interface. When the PHY has a valid link, the speed and duplex can be read from PHY_AUX_CTRL_STAT::SPEED_STAT and PHY_AUX_CTRL_STAT::FDX_STAT.

3.4.3.2 General Fault Indications

SparX-G5e is capable of detecting Far-End faults as reported by the auto-negotiation process. This type of fault is detected at the Far-End station and reported by the link partner through the auto-negotiation protocol. PHY_STAT::REMOTE_FAULT reports this event when it occurs.

SparX-G5e verifies the End Of Frame (EOF) sequence of all frames that are received. PHY_CTRL_STAT::EOF_ERR reports whether any errors are found.

3.4.3.3 10BASE-T Indications

The state of 10BASE-T link status is reflected in PHY_CTRL_STAT_EXT::LINK_10BT. This can also be determined in other ways: for more information, see "Link, Speed, and Duplex Indications," page 53. If the 10BASE-T carrier integrity monitor detects a break in a 10BASE-T link due to missing carrier, this is indicated in PHY_CTRL_STAT_EXT::LINK_10BT_DISCONNECT. It is possible, however, to disable this check by forcing link through PHY_CTRL_STAT_EXT::LINK_10BT_FORCE_ENA.

In 10BASE-T mode, the PHY can verify the length of transmissions and shut them down, if they are too long, using the Jabber function. If this condition occurs, the PHY reports that a transmission has been shut down using PHY_STAT::JABBER_DETECT. The Jabber check can be disabled through PHY_CTRL_STAT_EXT::JABBER_DETECT_DIS.

3.4.3.4 100BASE-TX Indications

PHY_STAT_100BTX::DESCRAM_LOCKED shows the status of the 100BASE-TX descrambler. If, for any reason, the descrambler detects an error, or it cannot lock in 100BASE-TX mode, this event is indicated by PHY_STAT_100BTX::DESCRAM_ERR.

For reference, PHY_STAT_100BTX::LINK_STAT reports whether a link is active in 100BASE-TX mode. This information is redundant, however: for more information, see "Link, Speed, and Duplex Indications," page 53. If an active 100BASE-TX link is broken, this is reported through PHY_STAT_100BTX::LINK_DISCONNECT.

PHY_STAT_100BTX::RECEIVE_ERR and PHY_STAT_100BTX::TRANSMIT_ERR report receive and transmit errors in 100BASE-TX mode.

PHY_STAT_100BTX::SSD_ERR and PHY_STAT_100BTX::ESD_ERR report Start-of-Stream and End-of-Stream Delimiter Errors in 100BASE-TX mode.

3.4.3.5 1000BASE-T Indications

PHY_STAT_1000BT_EXT::DESCRAM_LOCKED shows the status of the 1000BASE-T descrambler. If, for any reason, the descrambler detects an error, or it cannot lock in 1000BASE-T mode, this event is indicated by PHY_STAT_1000BT_EXT::DESCRAM_ERR.

For reference, PHY_STAT_1000BT_EXT::LINK_STAT reports whether a link is active in 1000BASE-T mode. This information is redundant, however. For more information, see "Link, Speed, and Duplex Indications," page 53. If an active 1000BASE-T link is broken, this is reported through PHY_STAT_1000BT_EXT::LINK_DISCONNECT.

PHY_STAT_1000BT_EXT::RECEIVE_ERR and PHY_STAT_1000BT_EXT::TRANSMIT_ERR report receive and transmit errors in 1000BASE-T mode, respectively.

PHY_STAT_1000BT_EXT::SSD_ERR and PHY_STAT_1000BT_EXT::ESD_ERR report Start-of-Stream and End-of-Stream Delimiter Errors in 1000BASE-T mode, respectively.

In 1000BASE-T mode, the PHY checks for Carrier Extension Error. If this event occurs, it is reported through PHY_STAT_1000BT_EXT::CARRIER_EXT_ERR. If the link partner is non-compliant to BCM5400, this is reported through PHY_STAT_1000BT_EXT::BCM5400_ERR.

In 1000BASE-T mode, the status of the local and the remote receiver are reported through LOCAL_RECEIVER_STAT and REMOTE_RECEIVER_STAT in the PHY_STAT_1000BT register.

The PHY counts the number of Idle Errors conditions in 1000BASE-T mode. This counter is located at PHY_STAT_1000BT::IDLE_ERR_CNT. In addition, in 1000BASE-T mode, the PHY also counts CRC errors. This counter is located at PHY_CTRL_EXT4::CRC_1000BT_CNT.

3.4.4 Parallel LED Output

SparX-G5e contains dedicated pins to drive four LEDs directly for each PHY port. All LED outputs are active-low. For information about power supply, see "LED Outputs," page 287.

Each LED pin can be configured to any of the 14 functional modes shown in the following table. Configuration is performed by assigning a particular mode to any of the PHY_LED_CTRL::LED_PIN[3:0]_MODE_CFG register fields.

Table 10. LED Functions

LED Function	Mode	LED Output	Description
Link/Activity	0000	1	No link established at any speed.
		0	Valid link at any speed.
		Blink(1,2)	Valid link at any speed and activity present.
Link1000/Activity	0001	1	No link in 1000BASE-T.
		0	Valid 1000BASE-T link.
		Blink(1,2)	Valid 1000BASE-T link and activity present.
Link100/Activity	0010	1	No link in 100BASE-TX.
		0	Valid 100BASE-TX link.
		Blink(1,2)	Valid 100BASE-TX link and activity present.
Link10/Activity	0011	1	No link in 10BASE-T.
		0	Valid 10BASE-T link.
		Blink(1,2)	Valid 10BASE-T link and activity present.
Link100/1000/Activity	0100	1	No link in 100BASE-TX or 1000BASE-T.
		0	Valid 100BASE-TX link or valid 1000BASE-T link.
		Blink(1,2)	Valid 100BASE-TX link or valid 1000BASE-T link and activity present.
Link10/1000/Activity	0101	1	No link in 10BASE-T or 1000BASE-T.
		0	Valid link in 10BASE-T or 1000BASE-T.
		Blink(1,2)	Valid link in 10BASE-T or 1000BASE-T and activity present.
Link10/100/Activity	0110	1	No link in 10BASE-T or 100BASE-TX.
		0	Valid 10BASE-T link or valid 100BASE-TX link.
		Blink(1,2)	Valid 10BASE-T link or valid 100BASE-TX link and activity present.
Reserved	0111	Undefined	Reserved.
Duplex/Collision	1000	1	Link established in half-duplex mode, or no link established.
		0	Link established in full-duplex mode.
		Blink(1,2)	Link established in half-duplex mode and collision present.

Table 10. LED Functions *(continued)*

LED Function	Mode	LED Output	Description
Collision	1001	1	No collision detected.
		Blink(2)	Collision detected.
Activity(3)	1010	1	No activity(3) present.
		Blink(2)	Activity(3) present.
Alternative Activity(3)	1011	1	No activity(3) present.
		Blink(2)	Activity(3) present.
Reserved	1100	Undefined	Reserved.
Serial	1101		For more information, see "Serial LED Output," page 57.
Force Off	1110	1	Force the LED off.
Force On	1111	0	Force the LED on.

1. The blink operation can be disabled for individual LEDs. For more information, see "LED Options in Parallel Mode," page 56.
2. The blink operation can be pulse-stretched. For more information, see "LED Options in Parallel Mode," page 56.
3. The Alternative Activity mode is tied to Activity, when PHY_LED_BEHAVIOR_CTRL::ALT_ACTIVITY_ENA is enabled. The Alternative Activity mode reflects receive activity, whereas the Activity mode reflects transmit activity. As a default, the Activity mode indicates both receive and transmit activity, and the LED output in the Alternative Activity mode is undefined.

Force LED modes can also be used with the V-Core CPU and the GPIO pins to provide general-purpose control logic for external LEDs or SFP ports. For example, these pins can easily be used to signal VeriPHY events on external LEDs (for example, cable short or open), to indicate speed downshift status, to control external SFPs, or to interface with external Power-over-Ethernet controllers (IEEE Std. 802.3af).

3.4.4.1 LED Options in Parallel Mode

In addition to the basic operation of the functional modes, several options are available to increase the flexibility of each LED output. To reduce power consumption, LED outputs can be configured to pulse at 5 kHz with a 20% duty cycle by enabling LED pulsing through PHY_LED_BEHAVIOR_CTRL::PULSING_ENA.

For the functional modes that define blinking, various changes can be made to the blinking operation:

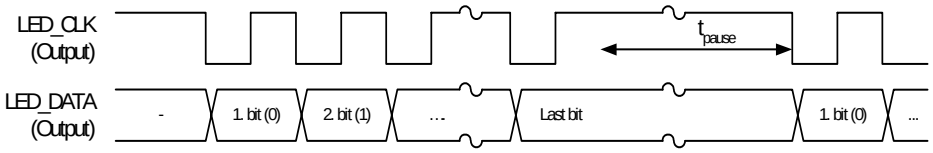
- Blinking frequency can be set through PHY_LED_BEHAVIOR_CTRL::BLINK_RATE_CFG.
- Blinking can be disabled on a per LED output basis. This is done by disabling the secondary combination, that is, activity or collision in Table 10. This is done through PHY_LED_BEHAVIOR_CTRL::COMBINATION_DIS.
- Pulse Stretched mode can be configured on a per LED output basis (see PHY_LED_BEHAVIOR_CTRL::PULSE_STRETCH_ENA). Then, instead of blinking, the current state of the LED output inverts for as long as the event is active (which normally causes blinking), but no less than the minimum amount of time defined by PHY_LED_BEHAVIOR_CTRL::BLINK_RATE_CFG. This mode guarantees that even very short "active" periods can be perceived by the human eye.

3.4.5 Serial LED Output

A serial LED function mode, which is available through PHY 0, provides access to most of the LED status signals for all the PHYs by continually transmitting these on PHY 0 LED outputs 0 and 1. Selecting the "Serial" LED function for PHY 0 LED outputs 0 and 1 activates this mode of operation; for more information, see "Parallel LED Output," page 55. The electrical specifications of the outputs in serial mode is equivalent to the parallel mode.

In serial mode, LED output 0 on PHY 0 acts as a data output and LED output 1 acts as the serial clock output. On these two outputs, SparX-G5e sends a single burst of status information and then pauses before repeating this process. A reader can be synchronized to this signal by observing the pause in between bursts of information. The burst consists of all the status bits of PHY 0, followed by all the status bits of PHY 1, followed by all the status bits of PHY 2, and so on, until the status for all PHYs has been transmitted. This process of a burst followed by a pause is illustrated in the following figure. For more information about timing parameters, see "Serial LED Output Timing," page 248.

Figure 7. Serial LED Output Functional Timing



The serial bit-stream outputs 12 LED status bits for each of the PHYs, as shown in the following table.

Table 11. Serial LED Output Sequence

Bit Position	LED Function Equivalent	Description
0	Link/Activity	See description in Table 10.
1	Link1000/Activity	See description in Table 10.
2	Link100/Activity	See description in Table 10.
3	Link10/Activity	See description in Table 10.
4	Reserved	Reserved.
5	Duplex/Collision	See description in Table 10.
6	Collision	See description in Table 10.
7	Activity	See description in Table 10.
8	Reserved	Reserved.
9	Tx_Activty	Transmit Activity.
10	Rx_Activity	Receive Activity.
11	Reserved	Reserved.

3.4.5.1 LED Options in Serial Mode

Just as in parallel mode, several options can be applied to the functional modes for increasing the flexibility of each serial LED bit. These options are configured on a per PHY basis.

For the functional modes that define blinking, various changes can be made to the blinking operation:

- The frequency of the blinking can be set through PHY_LED_BEHAVIOR_CTRL::BLINK_RATE_CFG.
- Blinking can be disabled by disabling the secondary LED combination, that is, activity and collision (Table 11.) This is done through PHY_LED_BEHAVIOR_CTRL::COMBINATION_DIS[0]. Note that in serial mode, the combination-disable configuration corresponding to LED output 0 applies to all bits of that particular PHY.
- Serial LED bits can be Pulse Stretched as in the parallel mode by setting the PHY_LED_BEHAVIOR_CTRL::PULSE_STRETCH_ENA[0] (for more information, see "LED Options in Parallel Mode," page 56). Note that in serial mode, the pulse stretch configuration corresponding to LED output 0 applies to all bits of that particular PHY.

In serial mode, all fields of register PHY_LED_BEHAVIOR_CTRL, other than the ones described previously, must be set to their default values.

3.4.6 VeriPHY Cable Diagnostics

SparX-G5e provides a comprehensive suite of cable diagnostic functions, which are available through the on-board processor. These functions have the ability to identify the cable length and operating conditions, and to isolate a variety of common faults that can occur on the Cat5 twisted pair cabling.

If a link is established on the twisted pair interface in 1000BASE-T mode, the VeriPHY cable diagnostics can run without disruption of the link or of any data transfer. However, if a link is established in 100BASE-TX or 10BASE-T, the VeriPHY cable diagnostics cause the link to drop while the diagnostics are running. After the diagnostics are finished, the link is reestablished. For an example of a working implementation of the VeriPHY functions, see the SparX-G5e PHY API.

The following functions are available.

- Coupling between cable pairs
- Cable pair termination
- Cable Length

3.4.6.1 Coupling Between Cable Pairs

Anomalous coupling between cable pairs can be caused by shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map. These conditions can all prevent the SparX-G5e device from establishing a link.

3.4.6.2 Cable Pair Termination

Proper termination of Cat5 cable requires a 100 Ω differential impedance between the positive and negative cable terminals. IEEE Std 802.3 allows for a termination of as large as 115 Ω or as small as 85 Ω. If the termination falls outside of this range, it is reported as an anomalous termination by the VeriPHY cable diagnostics. The diagnostics can also determine the presence of an open or shorted cable pair.

3.4.6.3 Cable Length

When properly terminated, VeriPHY reports the approximate cable length in meters for each of the four cable pairs A, B, C, and D.

3.4.7 Manual Power-Down Modes

SparX-G5e implements IEEE-specified manual power-down mode through PHY_CTRL::POWER_DOWN_ENA, which shuts down the entire PHY, leaving only registers access available. Alternatively, you can disable just the transmitter part of the PHY, and this powers down the analog parts of the transmit path (see PHY_BYPASS_CTRL::TX_DIS).

When re-enabling the PHY after using any of the manual power-down modes, the PHY transmitter must be powered up manually. This is done for each PHY that is re-enabled, using the PHY Initialization Sequence. For more information about the PHY Initialization Sequence, "Initialization Sequence," page 140.

3.4.8 Ethernet In-Line Powered Device Support

3.4.8.1 IEEE Std 802.3af (DTE Power Through MDI)

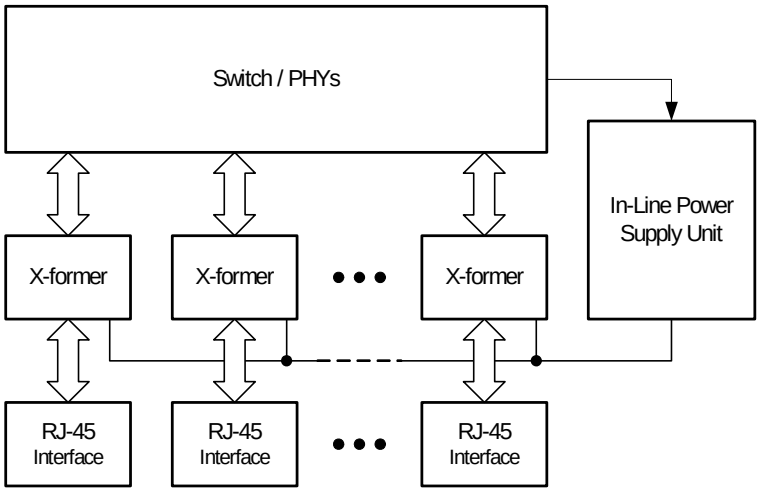
The SparX-G5e device is fully compatible with designs that are intended for use in systems that supply power to the DTE (Data Terminal Equipment) through the MDI (Media-Dependent Interface, or twisted pair cable), as specified by Clause 33 in IEEE Std 802.3af.

3.4.8.2 Cisco In-Line Powered Device Detection: an Overview

In addition, the SparX-G5e device supports the detection of Cisco In-Line Powered Devices as developed by Cisco Systems, and which is not part of IEEE Std 802.3af. Because many products from Cisco Systems that were developed prior to the ratification of IEEE Std 802.3af include support for this method, the SparX-G5e device supports detection of the Cisco Systems devices as well. This method is used for detecting in-line powered devices in Ethernet network applications.

SparX-G5e's in-line powered device detection mode can be part of a system that allows for IP-phone and other devices, such as wireless access points, to receive power from an Ethernet cable, similar to office digital phones receiving power from a PBX (Private Branch Exchange) office switch through the phone cable. This can eliminate the need for an IP-Phone to have an external power supply, because the Ethernet cable provides power. It also enables the in-line powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, and so on). Each of the PHYs can independently perform in-line power detection for devices complying with the Cisco Systems specification. This mode is disabled by default, and must be enabled for each PHY to perform in-line powered device detection. For more information, see *10/100 Ethernet In-Line Power Detection Algorithm* at the Cisco Systems Web site at www.cisco.com.

Figure 8. In-Line Powered Ethernet Diagram



In-Line Powered Device Detection (Cisco Method): Functional Implementation

This section describes the flow process that an Ethernet switch must perform to process in-line power requests made by a Link Partner (LP) capable of receiving in-line power.

1. The in-line powered device detection mode is enabled on each PHY setting PHY_CTRL_EXT4::INLINE_POW_DET_ENA and ensuring auto-negotiation is enabled (for more information, see "Auto-Negotiation," page 51). The PHY then starts sending a special Fast Link Pulse (FLP) signal to the LP.
2. The PHY monitors for the special FLP signal looped back by the LP. An LP device capable of receiving in-line power loops back the special FLP pulses when it is in a powered-down state. PHY_CTRL_EXT4::INLINE_POW_DET_STAT report the state of this detection process.
3. If the PHY reports that the LP needs in-line power, then the Ethernet switch needs to enable in-line power on this port external to the PHY.
4. The PHY automatically disables in-line powered device detection and changes to the normal auto-negotiation process.
5. If a link is not established, in-line power should be disabled to the in-line powered device external to the PHY. The PHY disables the normal auto-negotiation process and re-enables in-line powered device detection mode.

3.4.9 ActiPHY™ Power Management

In addition to the IEEE-specified power-down control bit PHY_CTRL::POWER_DOWN_ENA, the device includes an ActiPHY™ power management mode for each PHY. This mode enables support for power-sensitive applications, such as laptop computers with Wake-on-LAN™ capability. It uses a signal-detect function that monitors the media interface for the presence of a link to determine when to power down the PHY automatically. The PHY wakes up at a programmable interval and attempts to wake-up the link partner PHY by sending a burst of fast link pulse (FLP) over copper media.

The ActiPHY™ power management mode can be set at any time, on a per port basis, during normal operation by setting PHY_AUX_CTRL_STAT::ACTIPHY_ENA.

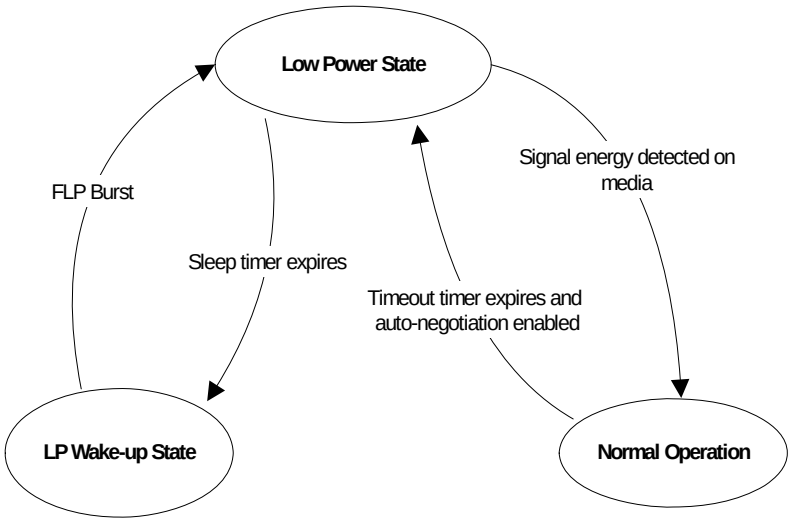
There are three PHY operating states when ActiPHY™ mode is enabled:

1. Low power state
2. LP Wake up state
3. Normal operating state (link up state)

The PHY switches between the low power state and LP wake up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. When the PHY is in the normal operating state and link is lost, the PHY returns to the low power state after the link status time-out timer has expired. After reset, the PHY enters the low power state.

When auto-negotiation is enabled in the PHY, the ActiPHY™ state machine operates as described. If autonegotiation is disabled and the link is forced to 10BT or 100BTX modes while the PHY is in the low power state, the PHY continues to transition between the low power and LP Wake up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state, even when the link is dropped. If auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

Figure 9. PHY Operating States



3.4.9.1 Low Power State

In the low power state, all major digital blocks are powered down.

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Auto-negotiation incapable (blind/forced) 100BTX-only link partner
- Auto-negotiation incapable (blind/forced) 10BT-only link partner
- Another PHY in Enhanced ActiPHY™ LP Wake Up state

In the absence of signal energy on the media pins, the PHY transitions from the low power state to the LP Wake up state periodically, based on the sleep-timer setting. The actual sleep time duration is randomized around the sleep-timer setting; the duration can range from 80 ms less than the setting to 60 ms greater than the setting. This is to avoid two linked PHYs in ActiPHY™ mode from entering a lock-up state. For more information about the sleep timer settings, see the PHY_AUX_CTRL_STAT register, Table 193, page 200.

3.4.9.2 LP Wake Up State

In this state, the PHY attempts to wake up the link partner. Up to three complete FLP (Fast Link Pulse) bursts are sent on alternating pairs A and B of the Cat5 media.

After sending signal energy on the relevant media, the PHY returns to the low power state.

3.4.9.3 Normal Operating State

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the link status time-out timer default of two seconds and then enters the low power state.

3.4.10 Advanced Test Modes

3.4.10.1 Ethernet Packet Generator (EPG)

For system-level debugging and in-system production testing, each PHY in the SparX-G5e device includes an Ethernet packet generator for 1000BASE-T testing. This can be used to isolate problems between the MAC and PHY and between a local PHY and remote link partner.

Caution This feature is intended for use with laboratory testing equipment or in-system test equipment only, and should not be used when SparX-G5e is connected to a live network.

To use the EPG, it must be enabled in PHY_1000BT_EPG1::EPG_ENA. This effectively disables the transmit channel and selects the EPG as the source for all data transmitted onto the twisted pair interface. For this reason, packet loss occurs if the EPG is enabled during transmission of packets from MAC to PHY. The MAC receive channel is still active when the EPG is enabled, however. If it is necessary to disable the MAC receive channel as well, this can be done by isolating the MAC and the PHY. For more information, see “Miscellaneous Test Setups,” page 65.

When PHY_1000BT_EPG1::EPG_RUN_ENA is enabled, SparX-G5e begins transmitting IEEE Std 802.3 Layer-2 compliant packets with a data pattern of repeating 16-bit words (as set in PHY_1000BT_EPG2::PACKET_PAYLOAD_CFG). The duration of the transmission is configured in PHY_1000BT_EPG1::TRANSMIT_DURATION_CFG.

The source and destination addresses for each packet, packet length, and inter-packet gap can be configured through the following fields:

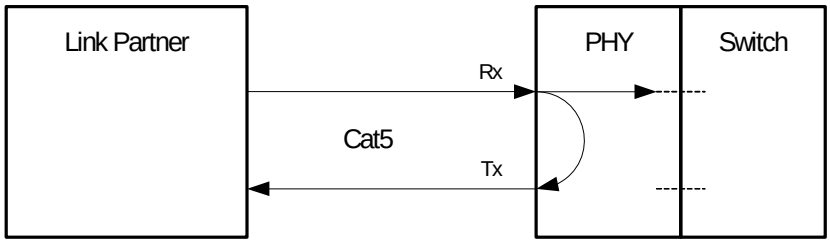
- PHY_1000BT_EPG1::SRC_ADDR_CFG
- PHY_1000BT_EPG1::DEST_ADDR_CFG
- PHY_1000BT_EPG1::PACKET_LEN_CFG
- PHY_1000BT_EPG1::INTER_PACKET_GAP_CFG

In addition, the EPG can be configured to generate a bad FCS (Frame Check Sequence). This is enabled in PHY_1000BT_EPG1::BAD_FCS_ENA.

3.4.10.2 Far-End Loopback

When enabled in PHY_CTRL_EXT1::FAR_END_LOOPBACK_ENA, the far-end loopback mode forces incoming data from a link partner on the current media interface to be retransmitted back to the link partner on the media interface, as shown in the following diagram. The incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored in this mode.

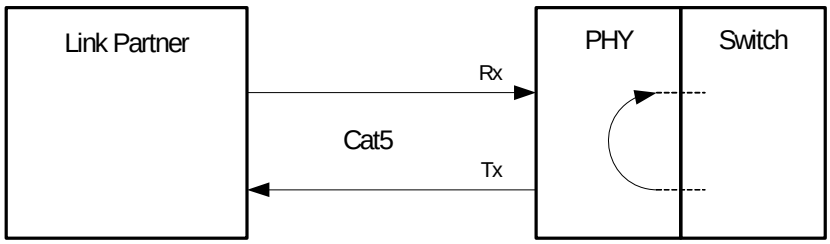
Figure 10. Far-End Loopback Block Diagram



3.4.10.3 Near-End Loopback

When near-end loopback is set in PHY_CTRL::LOOPBACK_ENA, the Transmit Data from the MAC interface is looped back as Receive Data to the MAC, as shown in the following diagram. In this mode, no signal is transmitted over the network media.

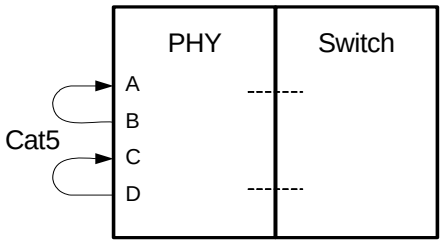
Figure 11. Near-End Loopback Block Diagram



3.4.10.4 Connector Loopback

Connector Loopback allows the media interface to be looped back externally. In this mode, the PHY must be connected to a loopback connector or a loopback cable. For twisted pair media, pair A should be connected to pair B and pair C to pair D. This loopback works at all speeds selected for the interface.

Figure 12. Connector Loopback for Twisted Pair Media



For 1000BASE-T connector loopback only, the following writes are required in the specified order.

- Master/slave configuration forced to master through PHY_CTRL_1000BT::MANUAL_CFG_ENA and PHY_CTRL_1000BT::MS_MANUAL_CFG.
- Enable 1000BASE-T connector loopback through PHY_CTRL_EXT2::CON_LOOPBACK_1000BT_ENA.
- Disable pair swap correction (for more information, see "Auto MDI/MDI-X Function," page 51).
- Disable auto-negotiation and force 1000BASE-T link in Full-Duplex (for more information, see "Auto-Negotiation," page 51).

3.4.10.5 Transmitter/Receiver Test Mode

In 1000BASE-T mode, the transmitter can be configured to transmit test patterns, as described in IEEE Std 802.3-2002, section 40.6.1.1.2. This is done by configuring test modes in PHY_CTRL_1000BT::TX_TEST_MODE for the PHY. When operating in any of the following test modes, the PHY should operate from a ±0.01% clock source.

Test Mode 1—Transmit Waveform Test

In this mode, the PHY should operate in master timing. The PHY continually transmits the following sequence of data symbols from all transmitters:

1. **+2** symbol followed by 127 **0** symbols.
2. **–2** symbol followed by 127 **0** symbols.
3. **+1** symbol followed by 127 **0** symbols.
4. **–1** symbol followed by 127 **0** symbols.
5. 128 **+2** symbols.
6. 128 **–2** symbols.
7. 128 **+2** symbols.
8. 128 **–2** symbols.
9. 1024 **0** symbols.

Test Mode 2—Transmit Jitter Test in Master Mode

In this mode, the PHY should operate in master timing. The PHY transmits the data symbol sequence **+2 –2** repeatedly on all channels.

Test Mode 3—Transmit Jitter Test in Slave Mode

In this mode, the PHY should operate in slave timing. The PHY transmits the data symbol sequence **+2 –2** repeatedly on all channels.

Test Mode 4—Transmit Distortion Test

In this mode, the PHY should operate in master timing. The PHY transmits the sequence of symbols generated by the scrambler generator polynomial, bit-generation, and level mappings as defined for "Transmit Distortion Test" in IEEE Std 802.3-2002, section 40.6.1.1.2.

3.4.10.6 Miscellaneous Test Setups

To avoid unexpected behavior in some of the PHY test configurations, it may be desirable to disconnect the PHY from the MAC and the switch. Enabling PHY_CTRL::ISOLATE_ENA isolates the PHY from the MAC so that no data passes between them.

To test the MAC and PHY in half-duplex mode, the PHY can be configured to assert collision when the MAC sends traffic. This is enabled in PHY_CTRL::COLLISION_TEST_ENA.

3.5 MAC Functionality and Setup

This section describes the configuration options and high-level functionality of the MAC used on each of the 5+1 ports.

The MAC supports 10/100/1000 Mbps in full-duplex mode and 10/100 Mbps in half-duplex mode. One of the MACs is attached to an external GMII or RGMII.

3.5.1 Reset

In register MAC_CFG, the reset fields PORT_RST, MAC_TX_RST and MAC_RX_RST are all by default held in reset state 1. PORT_RST controls the queue system of the port; the two other reset fields control the transmitter and receive domain of the MAC. They can all be written with the same register write, and must all be set and cleared after any MAC configuration change— such as speed, flow control mode, inter-packet gaps, and so on.

3.5.2 MAC Clocking Setup

The Transmit Clock selection is done by writing to MAC_CFG::CLK_SEL. For more information about the possible settings, see "MAC Configuration—MAC_CFG (Address 0x00)," page 161.

The MAC is enabled by writing 1 to register MAC_CFG fields TX_EN and RX_EN.

When using 1000 Mbps clock speed, or when using a PHY source transmit clock set at 1000 Mbps, MAC_CFG::GIGA_MODE must be set; otherwise it must be cleared.

The duplex mode is selected in MAC_CFG::FDX, where 0 = half-duplex and 1 = full-duplex.

For more information about resetting a port, see "Arbiter Empty—ARBEMPTY (Address 0x0C)," page 177.

The MAC supports frame lengths up to 9.6 kilobytes. The maximum length accepted by the MAC is configurable in the MAXLEN register.

3.5.3 Half-Duplex

A number of special configuration options are available for half-duplex (HDX) mode:

- Field MAC_CFG::WEXC_DIS determines whether or not the MAC backs off after an excessive collision has occurred. If set, backoff is disabled after excessive collisions.
- The value of MACHDXGAP::BACKOFFBIAS can be used to adjust the back-off time. If the register value is increased by 1, the backoff time is decreased by eight bit times. The correct value depends on the delay from the MAC to the line, so the default value should be used normally.
- Field MACHDXGAP::LCOLPOS adjusts the border between a collision and a late collision in steps of 1 byte. According to IEEE Std 802.3 section 21.3, this border is allowed to be on data byte 56 (counting frame data from 1); that is, a frame experiencing a collision on data byte 55 is always retransmitted, and it is never retransmitted on byte 57. For each higher LCOLPOS value, the border is moved 1 byte higher.
- The sum of MACHDXGAP::IFG1 and MACHDXGAP::IFG2 times the Rx to Tx IFG. IFG1 is the first part of half-duplex Rx to Tx inter-frame gap. Within IFG1, this timing is restarted if CRS has multiple high-low transitions (due to noise). IFG2 is the second part of half-duplex Rx to Tx inter-frame gap. Within IFG2, transitions on CRS are ignored.
- Field ADVPORTM::EXC_COL_CONT determines whether the MAC retransmits frames after an excessive collision has occurred. If set, a frame is not dropped after excessive collisions, but the backoff sequence is restarted. This is a violation of the standard, but it is useful in non-dropping half-duplex flow control.

3.5.4 External (R)GMII

MAC number 6 is connected to the external GMII port. The external interface supports GMII, MII-10/100 and RGMII-10/100/1000. This interface is controlled by fields found in the ADVPORTM register:

- EXTERNAL_PORT—Connects the MAC to the external GMII port.
- DDR_MODE—Selects RGMII mode on the external interface.
- INVERT_GTX/ENABLE_GTX—Selects operation of the GTX clock for the port.

When running a port in RGMII mode, the receive and transmit clocks must be delayed relative to the data. This can be done internally in SparX-G5e, using the GMIIDELAY register in the system block. The clock speed of the port must be set in MAC_CFG:CLK_SEL.

3.5.5 Shrinkable Inter-Frame Gap

IEEE Std 802.3-2002 allows clock differences up to ±100 ppm for the Rx and Tx clock on an Ethernet interface. A side effect of this potential clock difference is that an ingress stream of frames can be received faster than the same stream can be transmitted on a Tx interface. In port-to-port throughput tests with an offered load of 100%, this leads to frame drops in the queue systems because frames are received faster than they can be transmitted.

To circumvent this issue, hardware designers tend to use an oscillator with a clock that is precise and slightly faster than its nominal rate. This adds cost to the design and is not guaranteed to work as the Rx clock can still be faster.

SparX-G5e supports another way to address this problem. Each port has a mechanism to continuously estimate the clock difference between an ingress stream and an egress stream. In cases where the Rx is faster than Tx, the egress MAC adjusts the interframe gap of the egress frames, whenever needed, to equalize the clock differences. Effectively, this means the egress IFG is occasionally 11 bytes instead of 12 bytes. Note that the shrinkable interframe gap is only active for traffic patterns where frames can be dropped due to clock differences; in true congested patterns such as a many-to-one setup, the IFG is not reduced.

The obvious benefits of this approach are that there are no special hardware requirements because standard oscillators can be used, and it is guaranteed that the egress stream will be equal to the ingress stream, independently of the Rx clock. However, note that shrinking the IFG is a violation of the standard.

The shrinkable IFG is enabled on a per-port basis in ADVPORTM::IFG_PPM.

3.6 Frame Categorization

Each port has a frame categorizer that is responsible for processing each incoming frame to determine a number of properties affecting the forwarding through the switch. These are the tasks of the categorizer:

- CPU forwarding determination—Copy or direct frame to CPU.
- Frame dropping determination—Drop illegal frame types.
- Priority assignment—Assign one of four QoS classes to the frame.
- Link aggregation code generation—Generate an aggregation code based on flow information in the frame.
- DSCP remarking request—Determine whether DSCP remarking should be requested.
- VLAN classification—Extract VLAN information from the frame or use port-based VLAN (for more information, see "VLAN Operation," page 72).

The following sections describe each of the tasks in detail, and how these tasks can be configured.

3.6.1 CPU Forwarding

The CPU forwarding task determines which frames should be copied and which frames should be redirected to the CPU for further processing. Copying means that the frame is also forwarded to the front ports determined by the analyzer, whereas redirection means that the frame only goes to the CPU. Most of the frame types to be copied or redirected to the CPU are identified by the categorizer. Exceptions are the following frame types, which are identified by the analyzer:

- Frames to the switch's management MAC address.
- Frames with unknown or moved SMAC to be learned by the CPU.
- Frames to be mirrored to the CPU.

The categorizer recognizes many different frame types and reports the type to the analyzer. The analyzer uses the type code when deciding whether to send the packet to the CPU Capture buffer, based on analyzer configuration in the CAPENAB register. When the frame arrives in the Capture module, the CAPCTRL register found in the system block selects the correct capture queue for the frame.

Note that, in terms of frame priority for storing frames in the ingress queue system, frames of types possibly redirected to the CPU only (BPDUs, ALLBRIDGE, GARP and IGMP frames) always get the highest priority to preserve management traffic and control protocols. This can be disabled in the CAT_PR_MISC_L2 register, so that the priority is determined through the general prioritization algorithm instead.

The following table shows how different frame types affect the direction of frames to the CPU. The class code is transferred to the analyzer module, which uses the code to determine the set of egress ports to which each frame should be forwarded. For more information about the frame class codes, see "Categorizer Classes," page 82.

Table 12. Frame Classes

Frame Type	Condition	Class to Analyzer
Reserved Addresses (IEEE Std 802.1D 7.12.6)	DMAC = 0x0180C200000x (BPDUs and various Slow Protocols supporting Spanning Tree, Link aggregation, and Port Authentication)	CPU_ONLY_BPDU (MAC control frames are filtered by the MAC)
Reserved ALLBRIDGE address	DMAC=0x0180C2000010	CPU_ONLY_ALLBR
GARP Application Addresses (IEEE Std 802.1D 12.5)	DMAC = 0x0180C200002x	CPU_ONLY_GARP
ARP MAC broadcast	DMAC = BC, Type = ARP	CPU_COPY_ARPBC
IGMP	DMAC = 0x01005E000000 to 0x01005E7FFFFF, Type = IP, IP type IGMP	CPU_ONLY_IGMP
IP Multicast Data	DMAC = 0x01005E000000 to 0x01005E7FFFFF, Type = IP, non-IGMP, DIP outside 224.0.0.x	CPU_FLOOD_IPMC
IP Multicast Ctrl	DMAC = 0x01005E000000 to 0x01005E7FFFFF, Type = IP, non-IGMP, DIP inside 224.0.0.x	CPU_COPY_IPMC
Others	Others	CPU_NORMAL

3.6.2 Frame Dropping

The categorizer can request the ingress queue system to drop a frame. The CAT_DROP register can be configured to drop the following frames:

- Frames with a multicast source MAC address.
- Frames with a NULL source or destination MAC address (Address = 00:00:00:00:00:00).
- MAC control frames.
- Pause frames.
- Untagged frames (excluding the IEEE Std 802.1D reserved range, GARP addresses, and the Bridge Group Management address).
- Tagged frames.

Note that priority-tagged frames are treated as untagged frames. By default, null MAC addresses, control frames, and pause frames are dropped by the categorizer.

3.6.3 Frame Priority Classification

SparX-G5e features a flexible QoS classification algorithm. The categorizer looks for information up to Layer 3, and it includes support for both IPv4 and IPv6 DSCP and IEEE Std 802.1p. The frame QoS classes 0–3 are encoded in a two-bit value, where 3 is highest priority and 0 is lowest priority. In short, the following fields can be used for determining the priority:

- Port default priority
- VLAN tag User Priority
- DSCP (both for IPv4 and IPv6 packets)

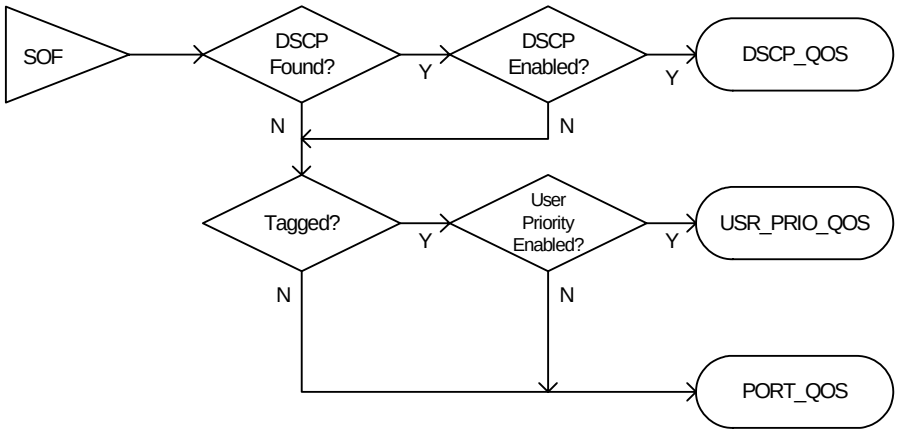
Frames marked for redirection to the CPU always get the highest QoS class, if enabled in CAT_PR_MISC_L2::CPU_HIGHQOS. For more information about the CPU forwarding capabilities, see "CPU Forwarding," page 68.

The set of configurable parameters related to priority determination is listed in the following table; the classification algorithm is shown in order of execution in Figure 13.

Table 13. Frame Priority Parameters

Registers	Description
CAT_PR_MISC_L2	Enable field for QoS class based on User priority (IEEE Std 802.1p) Configuration of port based QoS class. Enable field for giving CPU redirected frames highest QoS class.
CAT_PR_USR_PRIO	User Priority mapping table.
CAT_PR_DSCP_QOS	QoS class configuration for seven defined DSCP values (see CAT_PR_DSCP_VAL_0_3 and CAT_PR_DSCP_VAL_4_6) and for one QoS class for all undefined DSCP values.
CAT_PR_DSCP_VAL_0_3	Configuration of four DSCP values that can be recognized and used for prioritization
CAT_PR_DSCP_VAL_4_6	Configuration of three DSCP values that can be recognized and used for prioritization
CAT_PR_MISC_L3	Enable field for QoS class based on DSCP values

Figure 13. Categorizer Priority Classification Flow Chart



The following is an example of configuring parameters for prioritization:

All frames with DSCP = 7 are to get QoS class 2, and all other frames are to get class 0.

To do this, set CAT_PR_DSCP_QOS::DSCP_QOS_0 = 2, CAT_PR_DSCP_VAL_0_3:DSCP_VAL_:0 to 7, and CAT_PR_MISC_L2::PORT_QOS = 0.

3.6.4 Link Aggregation Code

The categorizer examines a frame to extract header information. The categorizer can be configured to generate a link aggregation code during this process. When the analyzer determines where to forward a frame, it uses the link aggregation code to select the correct port in an aggregation group. A key objective when selecting a port is keeping conversations between end stations, where the order of frames must be maintained, on the same port in the aggregation group.

It is the job of the analyzer to generate the final aggregation code used for selecting a port. For more information, see "Aggregation Processing," page 80. However, the categorizer can pass on to the analyzer a temporary aggregation code based on Layer 3 and 4 flow information – information that is known to be constant for frames within a given conversation. The register CAT_OTHER_CFG enables the use of IPv4 source and destination IP addresses, IPv6 flow label, and IPv4 source and destination port, independently of each other.

3.6.5 DSCP Remarking

DSCP Remarking enables rewriting of the DSCP field in IPv4 or IPv6 packets.

On ingress, DSCP remarking is controlled by CAT_PR_MISC_L3 and, on egress, by TXUPDCFG. Ingress may request certain remark actions, but the actual remarking is done in the egress port, and only if egress is enabled for it. Egress controls the actual new value to write to the DSCP field. Remarking only applies to IPv4 or IPv6 packets, and only to tagged frames if CAT_VLAN_MISC::VLAN_KEEP_TAG_ENA is cleared.

The following list describes the different DSCP values that, if enabled, can trigger a remark-request from the ingress side:

- Expedited Forwarding (RFC3246): Remarking requested if codepoint in frame equals 101110b.
- Assured Forwarding (RFC2475): Remarking requested if code point in frame equals any of the following Assured Forwarding (AF) code points:
  AF11 = 001010b, AF12 = 001100b, AF13 = 001110b, AF21 = 010010b,
  AF22 = 010100b, AF23 = 010110b, AF31 = 011010b, AF32 = 011100b,
  AF33 = 011110b, AF41 = 100010b, AF42 = 100100b, AF43 = 100110b.
- Class Selector (RFC2474): Remarking is requested if code point in frame equals any of the Class Selector (CS) code points. A CS code point is any of the eight code points in the range xxx000b.
- Zero code point: Remarking requested if codepoint in frame equals the zero code point.
- Other value: Remarking requested if code point in frame equals any other value than the values listed in the three groups above.

The remarking request is forwarded to the egress port, where the actual remarking is carried out by the rewriter module.

Four different remarking modes exist:

1. Map frame priority to AF code points. The four internal priorities are mapped to an AF code point as follows:
   0: AF12, 1: AF22, 2: AF32, 3: AF42
2. Map frame priority to CS code points. The four internal priorities are mapped to a CS code point as follows:
   0: 000000b, 1: 001000b, 2: 010000b, 3: 011000b
3. Remap frame priority, and then map to AF code points. The frame priority is remapped through CAT_GENERIC_PRIO_REMAP before remarking mode 1 is applied with the new priority.
4. Remap frame priority, and then map to CP code points. The frame priority is remapped through CAT_GENERIC_PRIO_REMAP before remarking mode 2 is applied with the new priority.

If DSCP remarking is enabled, the DSCP value in the frame is updated, as well as the IP checksum (IPv4) before transmitting the frame from the egress port.

3.7 VLAN Operation

The VLAN processing is shared between three blocks: the categorizer, the analyzer, and the rewriter.

- The analyzer handles the VLAN influence on frame forwarding. This is described in "Frame Analysis," page 74.
- The categorizer may remove tags from incoming frames and classify the frames to VLANs.
- The rewriter may insert tags on the egress side.

This section focuses on the categorizer and the rewriter. These are some of the features that are supported:

- Tagging and untagging of frames according to IEEE Std 802.1Q.
- Port based VLANs.
- Multiple VLAN tags with EtherType 0x8100.

A number of registers are used in the configuration of VLAN classification:

- CAT_VLAN_MISC: Enable bits for basic VLAN operation.
- CAT_PORT_VLAN: Configure the port based VLAN (CFI, User Priority, VID).
- TXUPDCFG: Basic operation regarding VLANs on the egress side of the device.

The following section describes the VLAN features in detail.

3.7.1 Ingress VLAN Classification

SparX-G5e always classifies incoming frames to a VLAN. In the VLAN-unaware mode, this classification does not influence the forwarding of the frame, whereas in VLAN-aware mode, the classification is used in the analyzer when making forwarding decisions. If one or more VLAN tags are present in a frame, the VLAN classification is always based on the outer tag in the frame, that is, the tag first seen when receiving the frame.

Two parameters in CAT_VLAN_MISC control the basic operation on the ingress side:

- CAT_VLAN_MISC::VLAN_TCI_IGNORE_ENA—If set, VLAN information is not retrieved from the frame, even if tagged. The frame is always classified as untagged.
- CAT_VLAN_MISC::VLAN_KEEP_TAG_ENA—If set, the VLAN tag is not removed from the frame before inserting the frame into the ingress queue system. Otherwise, the outer VLAN tag, if present, is removed from the frame and passed on to the analyzer in an Internal Frame Header (IFH). This parameter can be used for Q-in-Q access ports because, when setting VLAN_KEEP_TAG_ENA and configuring the switch to insert tags on the egress side, frames received with a single tag leave the switch with two tags. Likewise, it is possible to remove a tag by clearing VLAN_KEEP_TAG_ENA on the ingress port and configuring the egress port to transmit frames untagged.

The port based VLAN provides means of VLAN classifying untagged frames. For a normal VLAN-aware switch, the ingress VLAN membership classification is determined as follows:

- Untagged frame:
  - Assign to CAT_PORT_VLAN::VLAN_VID.
- Priority tagged frame (tagged frame with VID=0):
  - Use tag from frame but assign VID to CAT_PORT_VLAN::VLAN_VID. Place VLAN information in the Internal Frame Header.
  - The tag is stripped from the frame.
- Tagged frame (tagged frame with nonzero VID):
  - Use tag from frame and place tag information in the Internal Frame Header.
  - The tag is stripped from the frame.

The following pseudo-code shows more details about the ingress VLAN classification, including all relevant register references.

```
if (CAT_VLAN_MISC::VLAN_TCI_IGNORE_ENA || no_frame_tag_found) {
  /* Port VLAN */
  internal_frm_hdr.VID           = CAT_PORT_VLAN::VLAN_VID;
  internal_frm_hdr.CFI           = CAT_PORT_VLAN::VLAN_CFI;
  internal_frm_hdr.user_priority = CAT_PORT_VLAN::VLAN_USR_PRIO;
} else {
  if (frame_tag.VID == 0x000) {
    /* Priority tagged frame */
    internal_frm_hdr.CFI           = frame_tag.CFI;
    internal_frm_hdr.user_priority = frame_tag.user_priority;

    /* Port VLAN */
    internal_frm_hdr.VID = CAT_PORT_VLAN::VLAN_VID;
  } else {
    /* Tagged frame with VID */
    internal_frm_hdr.VID           = frame_tag.VID;
    internal_frm_hdr.CFI           = frame_tag.CFI;
    internal_frm_hdr.user_priority = frame_tag.user_priority;
  }
}
```

3.7.2 Egress VLAN Handling

The egress (Tx) VLAN handling is configured through the TXUPDCFG register. The egress port decides which frames to transmit tagged and which frames to transmit untagged. The following shows how the tagging or untagging is performed at the egress port (all register field references are to TXUPDCFG, unless otherwise stated):

- Do not tag frames (TX_INSERT_TAG=0):
  This is used, for example, when running SparX-G5e as a VLAN-unaware switch, or when the port is VLAN-wise configured as an access port.
- Tag all frames (TX_INSERT_TAG=1):
  This is used when the port is configured as a trunk port.
- Tag all frames except those with a specific VID (TX_INSERT_TAG=1):
  This is used when the port is configured as a hybrid port. Frames with a specific VID configured in TX_UNTAGGED_VID and enabled through TX_UNTAGGED_VID_ENA are not tagged.

When tagging frames, the tag information is taken from the Internal Frame Header. The following pseudo-code shows the egress VLAN classification.

```
if (TXUPDCFG::TX_INSERT_TAG &&
    !(TXUPDCFG::TX_UNTAGGED_VID_ENA &&
      internal_frm_hdr.VID==TXUDPCFG::TX_UNTAGGED_VID)) {
  insert_tag_in_frame=1;
} else {
   insert_tag_in_frame=0;
}
```

3.8 Frame Analysis

3.8.1 Tables in the Analyzer

The central analyzer module maintains a number of tables and masks. The following table lists the most important ones. For more information, see “Registers,” page 129.

Table 14. Basic Frame Analysis Data

Table/Register	Description
MAC Table	8192 stations learned by CPU or autolearned; each entry in the table is a MAC record.
VLAN Table	4096 masks with allowed egress ports for each VID, and a flag, VLAN_SRC_CHK, for checking the ingress port as being a member of the VLAN in which frames are received.
Source Port Masks	8 port masks with allowed egress ports for each ingress port.
Destination Port Masks	64 port masks with translation of logical port indexes to port masks.
Aggregation Port Masks	16 port masks with allowed egress ports for each aggregation key.
Flooding Port Masks	3 flooding port masks: one for unicast frames, one for IP multicast frames, and one for other multicast frames including the broadcast address.

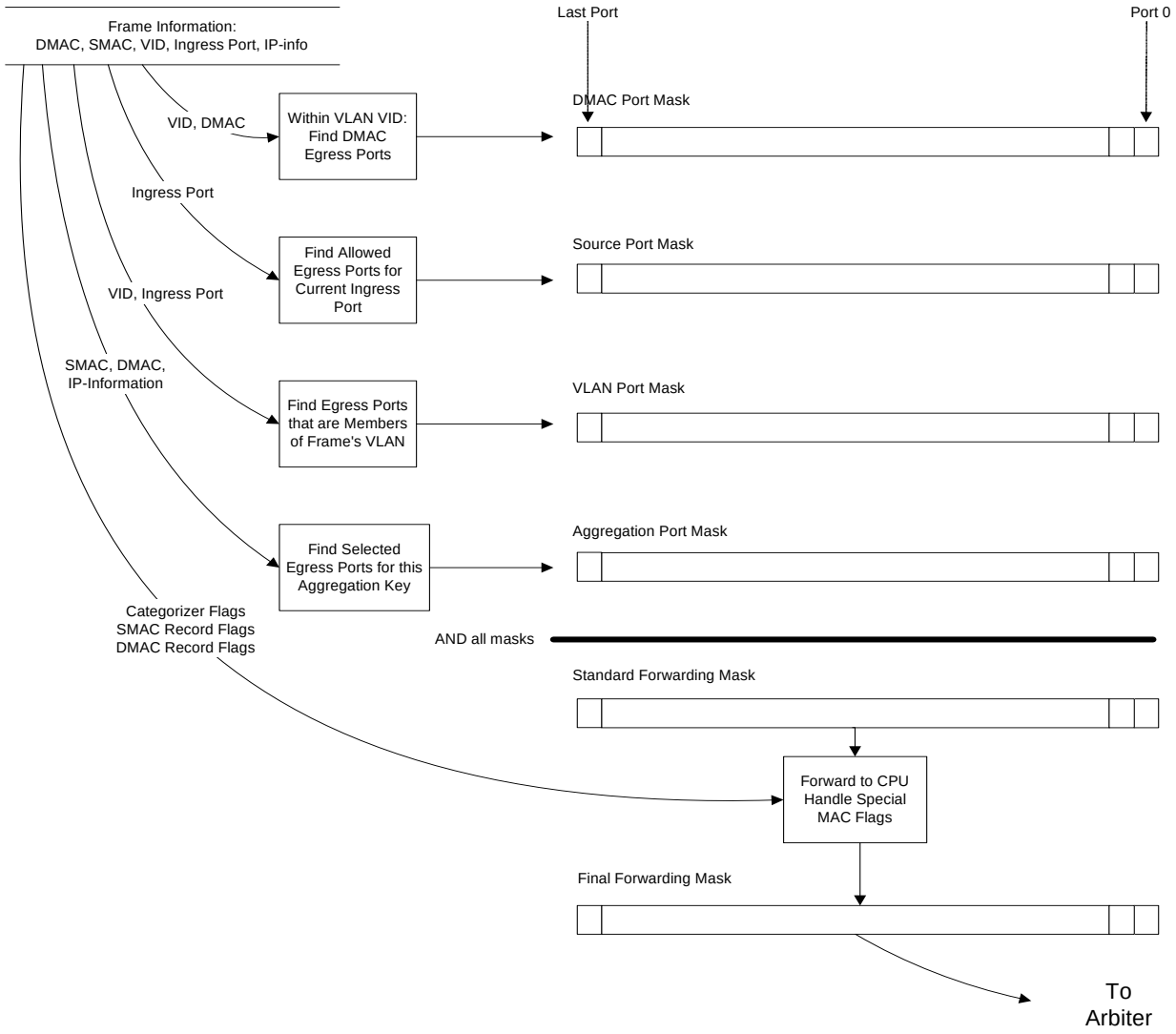
3.8.2 Analysis Overview

The end result of a frame analysis is the Forwarding Mask, containing the set of egress ports to which the analyzed frame is to be forwarded.

The forwarding decision is based on header information from the incoming frames, user configured tables, autolearned information, and the CPU class reported by the categorizer. For more information, see "CPU Forwarding," page 68.

The general flow is as shown in the following figure. Special cases (analysis exceptions) are not shown, but are described in "Exception Flags," page 81.

Figure 14. Frame Analysis



The final forwarding mask is the set of egress ports that get a copy of the frame. Basically, it is the ports that passed the four subanalysis steps shown in the preceding figure.

3.8.3 The MAC Table

SparX-G5e keeps track of which Destination MAC address belongs to which port by writing and reading an internal MAC address table. This table is used in the DMAC Analysis Block, which checks whether the DMAC address in the frame has been previously used as an SMAC address.

The MAC table consists of 8192 records, with the contents described in the following table.

Table 15. MAC Address Table

MAC Record Field	Description
MAC address	The 48-bit MAC address (matched at lookup).
VID	The 12-bit VID (matched at lookup).
DEST_IDX	Destination Mask number.
AGED_FLAG	Flag: aging has run since last learn of this address.
LOCKED	Flag: entry is locked. It is not aged out or overwritten.
VALID	Flag: entry is valid.
CPU_COPY	Exception Flag: copy frames destined for this DMAC to the CPU buffer.
FWD_KILL	Exception Flag: do not forward frames with this DMAC to any ports.
IGNORE_VLAN	VLAN Exception Flag: do not apply VLAN port mask for frames with this DMAC.

The table is automatically updated by an autolearning process, by a CPU-based learning process, or by direct manipulation from the CPU through register accesses. For more information, see "Direct MAC Table Access," page 76. The MAC address and VID are the identification of the station, the three flags hold the status of the entry, and the three exception flags are for special purposes, as explained later.

For autolearned ports, the destination index number is the port number it was learned from. It is used as a pointer into a table of 64 destination port masks, each translating this logical index number into a set of egress ports. In standard setups, only the destination port masks 0-4, 6 are used, and per default they are all configured to have only the port bit corresponding to their index set. So, if a station is learned on port 4, its record has 4 in the destination index, and when frames are sent to the station, destination port mask number 4 is used—which is a port mask with only the port 4 bit set.

3.8.3.1 Direct MAC Table Access

Apart from the more automated learning processes, it is possible to directly access the table to dump the contents or to write specific data at specific locations. This happens through the register interface.

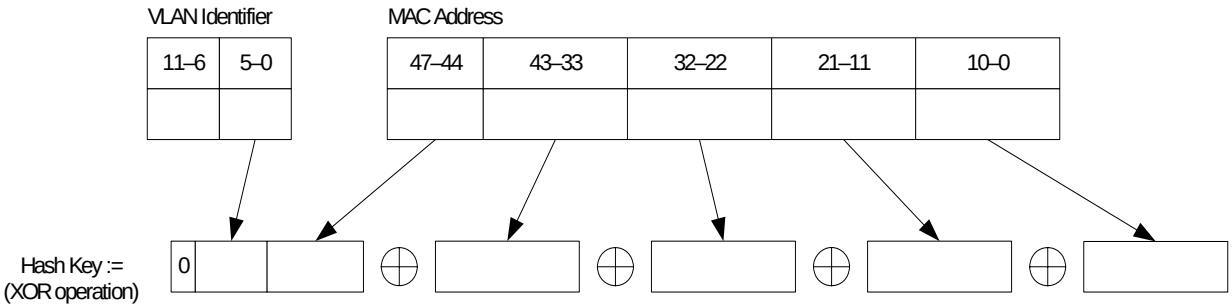
The MAC table is organized as a 2048 × 4 entry hash table. When accessing the table directly, the MACTINDX is first written with the desired record table position; and a Read Entry or Write Entry command is then issued through the MACACCESS register. To facilitate dumping or updating the whole table, each operation autoincrements the index.

Table 16. MAC Table Layout

Hash Key	0	1	2	3
0	MAC Record	MAC Record	MAC Record	MAC Record
1	MAC Record	MAC Record	(empty)	(empty)
2	MAC Record	(empty)	(empty)	(empty)
3	(empty)	(empty)	(empty)	(empty)
4	MAC Record	MAC Record	MAC Record	MAC Record
. . .	. . .	. . .	. . .	. . .
2047	MAC Record	MAC Record	(Empty)	(Empty)

Note To be found by the search engines, a MAC entry must be written into the correct hash chain. Therefore, when accessing the table for specific addresses, the table index must comply with the hash key formula, which basically is an XOR operation on most of the station identification (VID, MAC).

Figure 15. Hash Key Calculation



Example of the Hash Key Calculation

MAC address 00-00-12-34-56-78, in VID 15 has the hash key = XOR (0x0F0, 0x000, 0x048, 0x68A, 0x678) = 0x04A = 74 decimal.

Every time the search engines look up this address, hash chain 74 is searched.

The frame analysis process reorders each of the chains internally. To be able to read out all four entries of a chain while the analysis engine is operating, a chain shadow register can be enabled through the MACTINDX register. When using this register, only reading bucket 0 causes a physical read from the table, and buckets 1–3 are stored in a shadow chain. For more information, see the register description.

3.8.3.2 Shared or Independent VLAN Learning

By default, learning in SparX-G5e is Independent VLAN Learning (IVL).

IVL requires a MAC table entry to match exactly for both the MAC address and the VID. This implies that a MAC address that is learned in one VLAN cannot be used for forwarding by other VLANs; the other VLANs must learn the MAC address in their own VLAN.

The device also supports Shared VLAN Learning (SVL) where a MAC table entry is shared among a group of VLANs. For shared VLAN learning, a MAC address and a Filter Identifier (FID) define a unique learned entry. The FID may then map to a set of VIDs.

The AGENCTRL::FID_MASK controls the shared learning function. Bits set in the 12-bit FID_MASK mask out the corresponding bits in the VID. Therefore, the FID used for learning is given as FID = VID AND (NOT FID_MASK). As a result, all VIDs mapping to the same FID share VLAN learning.

If the FID_MASK is cleared, Independent VLAN Learning is used.

Examples:

Setting the FID_MASK to 0x0FF means that bits 7-0 in the VID are insignificant when looking up addresses in the database. Therefore, all the VIDs from 0 to 255 share one sub-database, the VIDs from 256 to 511 share another sub-database, and so on.

Setting the FID_MASK to 0x800 means that bit 11 is insignificant when looking up addresses in the database. Therefore, VID 0 and VID 2048 share a sub-database, VID 1 and VID 2049 share a sub-database, and so on.

Setting the FID_MASK to 0xFFF means that all bits of the VID are insignificant. Full shared VLAN learning is used. With the FID_MASK set to all ones, all VID bits are dont cares, and all VLANs use the same database.

3.8.4 Automatic Learning from Incoming Frames

Learning of stations is done automatically, if enabled for the ingress port. The learning process inserts an entry into the MAC table where:

- MAC = source MAC address from frame.
- VID = Source VID from frame (or PVID if untagged).
- DEST_IDX = ingress port number.
- AGED_FLAG = false, LOCKED = false, VALID = true.
- Flags IGNORE_VLAN, CPU_COPY, FWD_KILL are as configured in the AGENCTRL register.

The learning occurs at wire speed on every frame received. Regardless of a station already being present in the table, the learning mechanism is still activated. In this aspect, a station is learned every time it is seen as a source address.

The learning can be made dependent on the port being a member of the VLAN that the frame is received in, by setting the VLAN_CHK flag in the ADVLEARN register.

3.8.5 Manually Manipulating MAC Table Entries Through the CPU

MAC table entries can also be manually manipulated through the CPU Interface. Here, the CPU has full control over the flags and destination index inserted. This can be used for setting up permanent stations or multicast groups, where the locked flag must be set. In addition, it is used for CPU Based Learning. For more information, see "CPU-Based Learning," page 87.

When setting up a permanent station on a port, the CPU can write an entry with the locked and valid bits set, and with the destination index pointing to the port where the station is permanently attached.

When setting up a multicast group, an unused destination port mask is first allocated. It is used to remember the set of egress ports that belong to the group. After that, an entry is created in the MAC Table with the locked and valid bits set, and the destination port index pointing to the allocated destination port mask.

3.8.6 Unlearning/Aging

Aging is performed by writing an AGE command to the MAC Table Command register (MACACCESS), which subsequently causes the analyzer to run through all entries. In such an aging pass, one of two things happens to each entry: if the aged flag is set, the entry is cleared; if the aged flag is clear, the flag is set. The only exceptions to this procedure are locked entries, which are not modified. This means that all nonlocked entries that have not been relearned between two aging passes are removed.

Immediate unlearning of single MAC addresses is done by issuing a Forget to the MACACCESS register. For more information about the Forget operation and other MAC table operations, see "MAC Table Command—MACACCESS (Address 0xB0)," page 186.

3.8.7 Frame Forwarding Decision

The analysis of where to send a frame is done in four separate steps; for more information, see Figure 14, page 75. Each of these steps takes different conditions into account, as explained in the following sections.

3.8.7.1 DMAC Processing

This block finds the possible egress ports based on the DMAC and VID found in the frame. The MAC table is searched for an entry with matching VID and DMAC, and the output mask from this step is the destination port mask pointed to by the DEST_IDX found in the record. If the entry cannot be found, one of the globally configured Flooding Masks is instead returned, causing the frame to be forwarded to all the ports that have their corresponding bit set to 1 in the Flooding Mask.

3.8.7.2 VLAN Processing

The VLAN processing step looks up the allowed set of egress ports for the reported VID. The mask containing this information is taken from a configured table of records (VLAN Table). By default, this table is set to all-ones in all records, meaning that all ports are members of all VLANs. Each VLAN in the table can also be marked with the requirement that the ingress port must be a member of the VLAN if ingress frames are to be forwarded from this port. If this flag VLAN_SRC_CHK is set, and the ingress port's bit is not set in the given VLAN Table entry, the resulting mask from this step is all-zeros, that is, the frame is not forwarded to any port.

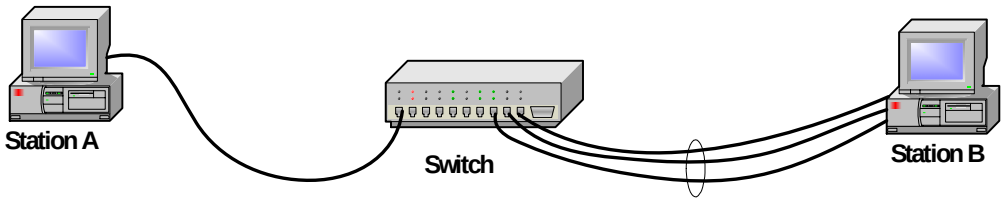
3.8.7.3 Source Port Processing

A frame must never be forwarded to its ingress port, as this results in network loops. This step ensures that this cannot happen. The ingress port number is used as an index into a table of eight port masks, each containing the set of egress ports to which a frame from any of the ingress ports may be forwarded. By default, every port bit in every mask of this table is set to 1, except the bit corresponding to each port's number. The source port masks can also be used to facilitate VLANs only defined by the switch port at which the frames are received (port grouping or port based VLANs).

3.8.7.4 Aggregation Processing

Link aggregation is a method of logically grouping a set of ports so that two network stations can be interconnected using multiple links. This method is used to create larger bandwidths between network nodes. All stations learned in a group of ports must be able to receive frames from all connections in the group. Also, the stations learned on any port in the group must be able to correctly forward frames to any other port in the group – like station B in the following figure.

Figure 16. Aggregation Example



Some of the port masks mentioned previously must be set to reflect the groups:

- The source port masks (SRCMASKS): For each port, this mask must be set so that an ingress port in a group cannot forward to any of the other ports in the same group.
- The destination port masks (DSTMASKS): This mask must be set so that a station learned on a port in a group can receive frames from all ports in that group.

When using link aggregation, the aggregation port masks (AGGRMSKS) are used to guarantee that any one frame is only transmitted to one port within a group. To achieve this, SparX-G5e calculates an aggregation key with a value between 0 and 15 for every frame received. The value is calculated in one of six ways, as determined by the AGGRCTRL register:

- The four least significant bits of the Source MAC Address (SMAC).
- The four least significant bits of Destination MAC Address (DMAC).
- The four least significant bits of (SMAC XOR DMAC).
- The four least significant bits of (SMAC XOR DMAC) XOR IP-information.
- IP-information.
- A pseudo-random number between 0 and 15 that directly selects which aggregation mask to use.

IP-information is a 4-bit code, generated by the categorizer, which may use IP information, such as source and destination IP addresses, TCP/UDP source and destination port numbers for IPv4 packets, and flow labels for IPv6 packets. For more information about the code generated by the categorizer, see "Link Aggregation Code," page 71.

The pseudo-random number approach is useful for networks where high utilization of aggregated links is important and where frame ordering within conversations can be neglected.

After it is calculated, the aggregation key is used as an index into a table of 16 aggregation port masks. In a nonaggregated setup, these masks are set to all-ones (the default value), but when setting up one or more aggregated groups, the masks must be configured such that only one port bit is set in each group.

Briefly, aggregation works like this:

1. SMAC/DMAC/IP-information are mapped into an aggregation key.
2. The aggregation key points to one of 16 aggregation port masks.
3. The selected aggregation port mask shows which port in the group should get the frame.

3.8.8 IP Multicast Groups

IP multicast MAC-table entries are handled in a special way. Each IP multicast entry can be inserted in the MAC table with its own unique group port mask, because they do not use the destination port mask table used by other entries.

When inserting an IP multicast MAC address into the MAC table, the procedure is:

1. Set IPMCACCESS::IPMC_EN = 1
2. Set IPMCACCESS::IPMCPORTS = group port mask for this entry
3. Set MACLDATA = 24-bit LSB of MAC address
4. Set MACHDATA::VID = VLAN ID for this entry
5. Set MACACCESS::LOCKED = 1, MACACCESS::MAC_TBL_CMD=LEARN
6. Set IPMCACCESS:IPMC_EN = 0

Note, the most significant 24 bits of the IP multicast MAC address (0x01005E) are implied and do not need to be programmed.

When reading the MAC table, an IP multicast entry is recognized by having both the LOCKED and AGE_FLAG bits in the MACACCESS register set. When reading the IP multicast entry with IPMCACCESS:IPMC_EN set, the group port mask is returned in IPMCACCESS::IPMCPORTS.

3.8.9 Exception Flags

In the preceding sections regarding the analyzer, only the most simple analysis cases have been explained. Some exception flags exist; for more information, see "The MAC Table," page 76. Together with the class reported by the categorizer on the ingress port, the exception flags can alter the way the masks are ANDed together.

Each entry in the MAC table has three exception flags:

- IGNORE_VLAN: The VLAN port mask is not ANDed with the forward mask.
- FWD_KILL: The destination port mask is set to all-zeros.
- CPU_COPY: Frames for this address are copied to the CPU capture buffer.

Entries that have been autolearned have their exception flags set to the configured learn flags found in the AGENCTRL register. CPU-learned entries have their exception flags set individually at the insert

operation. During analysis, the flags found in the MAC record are used if the lookup succeeded. Otherwise, flooding flags (also found in the AGENCTRL register) are used.

Examples of the use of these exceptions are:

- Frames with a reserved management MAC address are to be sent to the CPU and not elsewhere.
- Frames for a specific end station must be filtered.

In the first case, an entry from the CPU with DMAC = management MAC address, VALID = LOCKED = 1, FWD_KILL = 1, CPU_COPY = 1, is inserted. An entry must be inserted for each VLAN the frame can be received in.

In the second case, a permanent entry with DMAC = end station MAC address, VID = the VLAN in which the station was found, VALID = LOCKED = 1, FWD_KILL = 1, CPU_COPY = 0, is inserted.

Both the flags for the SMAC address and DMAC address are used for exception flags per default. This can however be disabled in the ANALYZER::AGENCTRL register.

3.8.10 Categorizer Classes

The final special case of the analysis flow is the Categorizer Class reported by the Categorizer block on the ingress port. Four different classes exist where the default class is CPU_NORMAL. When this is reported, no change is made to the analysis flow as it has been described above. If the CAPENAB register is configured for reacting on specific frame types, the frame is either sent to the Capture module only (CPU_ONLY_xxx types), copied to the Capture module (CPU_COPY_xxx types), or flooded to the IP multicast flooding mask when DMAC is unknown (CPU_FLOOD_IPMC).

3.8.11 Flooding Storm Limitation

The analyzer contains an algorithm for limiting the amount of flooding through the switch. It is possible to limit the rate of unicast, multicast, and broadcast flooding separately, only allowing a rate of approximately 1 to 255 kiloframes per second of flooding. It is handled through the STORMLIMIT register, where the rate for each traffic class (unicast, multicast, and broadcast) can be set, as well as the maximum burst of flooding exceeding the rate. For instance, if STORMLIMIT::MAXBURST is 1 and the rate is set to 2 kiloframes per second, a flooded frame does not allow any further flooding until 2 ms has passed.

Default, there are no limitations on the flooding capabilities.

3.8.12 Port Mirroring

The frame analysis engine has an option to mirror all frames either:

- Belonging to a specific VLAN, or
- Received on specific ports

The target port number is configured in the AGENCTRL register, and the source number (VLAN or port) is set in the VLAN table and source port masks. The CPU capturing can also be mirrored, which means that all frames destined for the CPU can be forwarded to the mirror port also. This is also set in the AGENCTRL register.

3.9 CPU Frame Transmit and Receive

Through the CPU interfaces of the device, it is possible to transmit and receive frames to and from the front ports. All three CPU interfaces (SI, PI, ICPU) can be used for frame handling, as the access to frame data is done through dedicated registers found in the port, and the CPU Capture area. Only the utilized CPU interface limits the speed of the frame transfer.

This section describes:

- The Internal Frame Header, with which all frames internally are prepended.
- The capturing mechanism used for reading out frames through the CPU interfaces.
- The redirection options, determining which frames to capture.
- Some advanced topics regarding frame capturing.
- The procedure used for transmitting frames through the CPU interfaces.

3.9.1 Internal Frame Header

All frames within the device are prepended with an 8-byte header. When transmitting frames through the CPU interfaces, such a header must be written before the actual frame data, and when reading out frames, the first 8 bytes is the header. The header holds information about the frame, such as frame length and VID for the frame.

Figure 17. Internal Frame Header

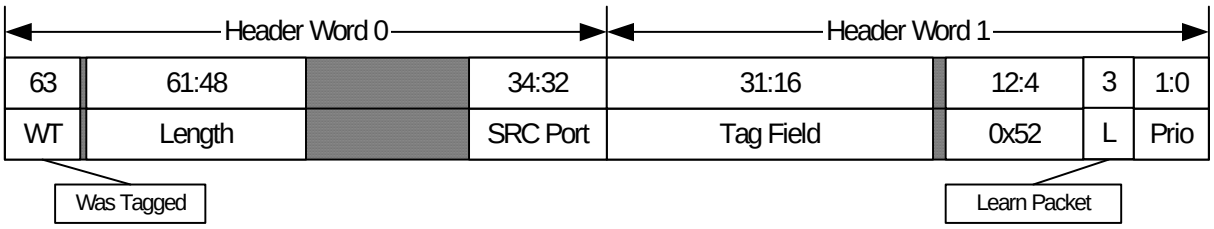


Table 17. Details About the Internal Frame Header

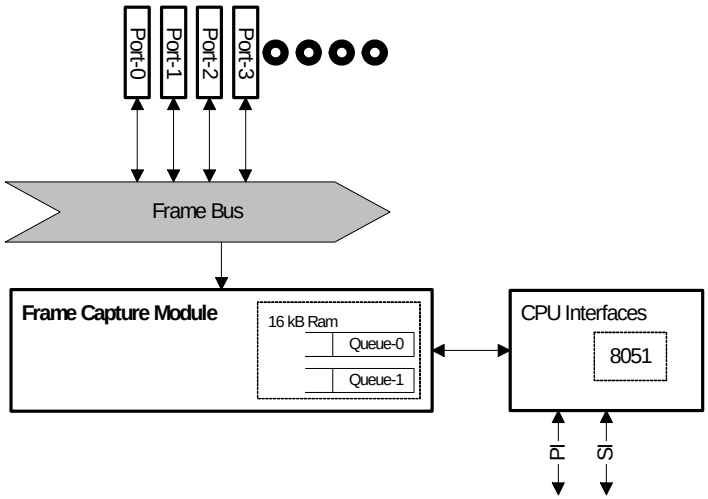
Field	Bits	Size	Description
WT	63	1	The frame was tagged upon reception, and the tag has been removed from the following frame data.
Length	61:48	14	The frame length including CRC, excluding the tag if WT=1.
SRC Port	34:32	5	The port number from which this frame was received (0-7).
Tag Field	31:16	16	The tag information found in the frame, or the fallback information if the frame was not tagged. For more information, see “Frame Categorization,” page 68.
0x52	12:4	9	This field is a magic signature. It should be verified upon frame readout.
LPA	3	1	The SMAC within this frame is a subject for learning.
Prio	1:0	2	The categorizer assigned priority for this frame.

When transmitting frames through the CPU interfaces, only the length and signature fields should be set correctly, and the rest should be zero. Transmitted frames are not modified on their way out, except for getting their CRC field recalculated. If a frame for transmission must be VLAN tagged, it must therefore be included in the written frame data.

3.9.2 Frame Capturing

A capture module is present within the SparX-G5e device. The capture module has a 16-kilobyte RAM for frame storage and supports two CPU queues. When configured, frames with specific properties can be stored in the capture queue system for later reading by the CPU. The following figure shows an overview of the CPU capture module.

Figure 18. CPU Capture Module



Through interrupts or status register polling, the CPU is notified when frames are present in any of the CPU queues in the capture module. The memory is accessed through a window, where only 2 kilobytes from each queue can be seen at a time (see Figure 19). The window is auto-aligned with the first unread frame, so that whenever a frame in queue 0 is ready:

- Register CPU_CAPT::0::FRAME_DATA[0] reads out bits 63–32 of the header of the first frame.
- Register CPU_CAPT::0::FRAME_DATA[1] reads out bits 31–0 of the header.
- Register CPU_CAPT::0::FRAME_DATA[2] returns the first 4 bytes of the DMAC of the first frame.
- Register CPU_CAPT::x::FRAME_DATA[y] returns 4 bytes from offset x × 1024 + 4 × y – 8 (where x is 0 or 1).

The same setup goes for queue 1, except for the window starting at CPU_CAPT::2::FRAME_DATA[0].

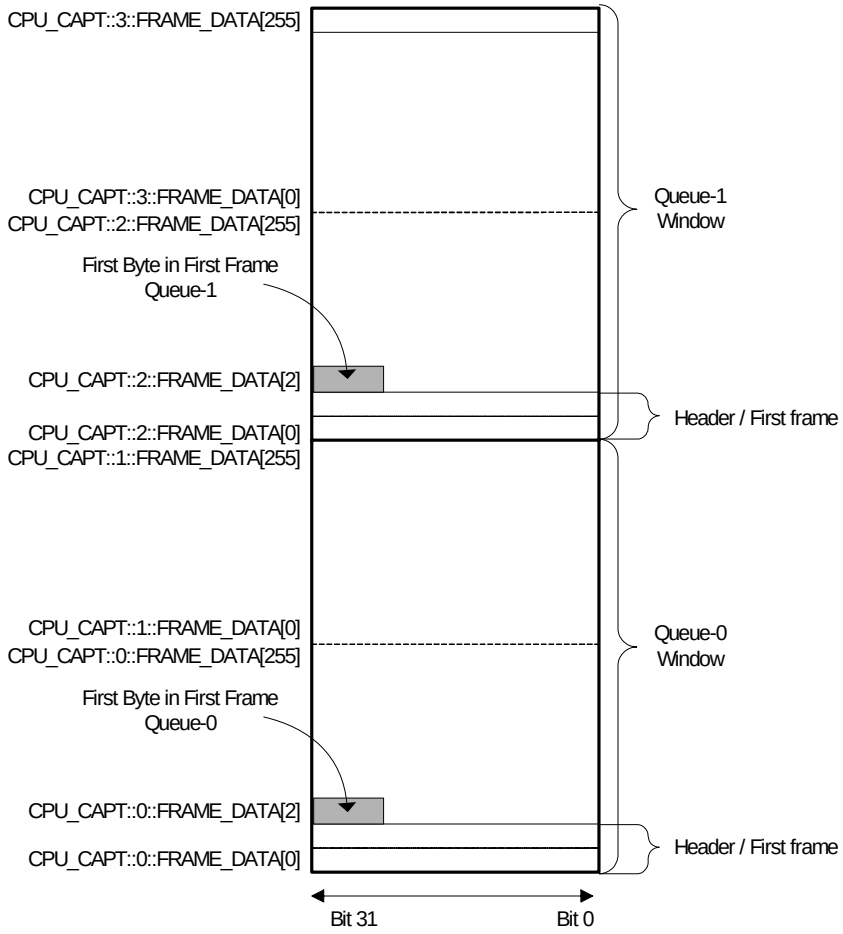
The CPU window can only read 2 kilobytes at a time. For captured frames larger than 2 kilobytes, the frame must be read as a number of 2-kilobyte frames, where the CPU window is moved forward through the frame. The CPU window is moved by writing a pseudo-frame length to the internal frame header and then releasing the frame. The CPU window moves the number of bytes specified by the pseudo-frame length, and the next part of the frame is ready for reading.

When a frame has been read, it is released from the memory by writing a release command to CPU_CAPT_CTRL::4::CAPREADP for queue 0 or CPU_CAPT_CTRL::6::CAPREADP for queue 1.

In the system register group, the CAPCTRL register configures and holds status for most of the capture-related information.

- Queue 1 is enabled by allocating memory through QUEUE1_MEM. Memory can be allocated in steps of 1 kilobyte. Queue0 is automatically allocated the remaining part of the 16 kilobytes. By default, only queue 0 is enabled with all 16 kilobytes of memory allocated.
- The two IRQ pins can be configured to signal when frames are present in the capture RAM.

Figure 19. CPU Queue Memory



3.9.3 Redirection Options

Through various configuration options, frames with specific properties can be redirected or copied into the CPU capture module. Basically, there are three groups of frames that can be redirected; frames for CPU controlled learning, frames used in software protocols running in the CPU, and frames for the MAC address assigned for switch management. In the CAPCTRL register, it can be configured which CPU queue different kinds of frames should be enqueued to. By default, all frames are assigned to queue 0 (which also has been assigned all of the memory in the capture module).

3.9.3.1 CPU-Based Learning

Station learning or move can be configured in the ADVLEARN register found in the Frame Analyzer block. One option is to set the CPU_LEARN flag to forward all such frames to the capture module. By also setting the AUTO_MODE flag to false, the MAC table can be completely controlled by the CPU. The frames for learning must be read out from the capture module, and a MAC entry can be added through the PI interface, as described in "Frame Analysis," page 74.

The CPU queue used for learning frames is set in CAPCTRL. The header of the frame contains the information about whether a frame is a target for learning.

3.9.3.2 Software Protocols

The categorizer of each port can be set for recognizing frames belonging to standard protocols with reserved MAC addresses, such as BPDUs, GARP and IGMP frames. For more information, see "CPU Forwarding," page 68. The target CPU queue is also configured in the categorizer registers.

3.9.3.3 Management Frames

When running switch management over the network, the software must be assigned a MAC address as its end station address on the network. All frames for this address must therefore be redirected to the CPU capture buffer. This is done by adding a MAC entry with this specific address, and the CPU_COPY flag set. For more information, see "Exception Flags," page 81.

3.9.4 Advanced Capture Options

3.9.4.1 Learn Truncation

When CPU-based learning is used, having the first segment of the frame present is sufficient when conducting the MAC learning process. As a result, you can configure all frames for learning to be truncated to 64 bytes. In this case, the frame length in the header is adjusted to 64 bytes also. It is then not possible to read the incoming frame length. The truncation is enabled in the CAPCTRL register.

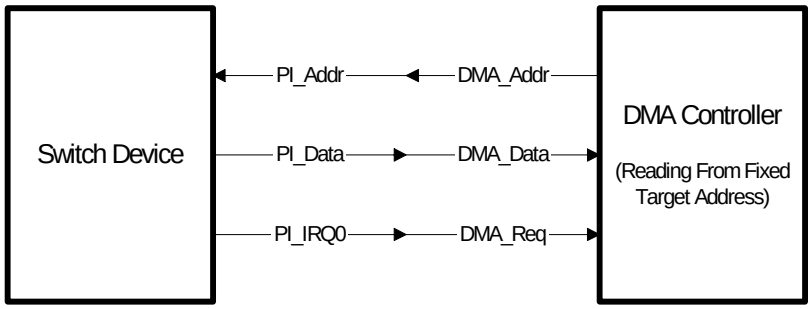
3.9.4.2 DMA Addressing

It is possible to access all of the capture memory by reading the same address repeatedly, which is useful when attaching DMA controllers to the PI interface. This is configured by setting the FIFO_MODE flag in CAPCTRL. When this is used, queue 0 is read only at address CAPTURE::0::0, and no frame release command should be used. When all of a frame has been read out, and no more frames are present, the CAPCTRL::QUEUE0_READY flag goes low, and no further readouts are allowed.

The above also applies to queue1, which is read at address CAPTURE::2::0.

An example of a simple DMA connection is shown in the following figure.

Figure 20. DMA Connection



3.9.5 CPU Frame Transmission

Frames can be generated on each of the ports by enqueueing data into each of the port queue systems. This is done by writing all of the frame, including Internal Frame Header, through the CPUTXDAT register on the port. The size of frames sent from the CPU must be a minimum of 64 bytes, so padding must be included with frames that are less than 64 bytes. An even number of writes must always be performed, but the real frame length must be written in the header (for more information, see "Internal Frame Header," page 84).

Therefore, a 67-byte frame requires 20 register writes (67 bytes + header = 75 bytes ~ 19 × 32-bit words). After all the writes have been performed, a CPU_TX command is given through the MISCFIFO register of the port.

The CPU transmit queue takes precedence over all other transmit queues on the port, which ensures that frames from that queue are transmitted quickly.

Each of the data writes into the queue system are, under most circumstances, performed faster than the speed of the CPU interface involved. However, under congested scenarios, where the queue system can be busy, it may take longer. This can be handled in two ways; either by polling for readiness between every two writes (Table 18), or by polling for write errors after the whole frame has been written (Table 19).

Table 18. CPU Transmit Operation Through Ready Polling

```
cpu_write PORT::no::CPUTXDAT length<<16; /* MS Header word */
cpu_write PORT::no::CPUTXDAT 0x520;      /* LS Header word */

while (cpu_read PORT::no::MISCSTAT & 0x100); /* Wait write */

for(i=0; i<int((length+7)/8); i++){
  cpu_write PORT::no::CPUTXDAT frame_data(i*8 to i*8+3);
  cpu_write PORT::no::CPUTXDAT frame_data(i*8+4 to i*8+7);
  while (cpu_read PORT::no::MISCSTAT & 0x100); /* Wait write */
}
cpu_write PORT::no::MISCFIFO 1; /* Send frame */
```

Table 19. CPU Transmit Operation Through Overflow Check

```
cpu_write PORT::no::CPUTXDAT length<<16; /* MS Header word */
cpu_write PORT::no::CPUTXDAT 0x520;      /* LS Header word */

for(i=0; i<int((length+7)/8); i++){
  cpu_write PORT::no::CPUTXDAT frame_data(i*8 to i*8+3);
  cpu_write PORT::no::CPUTXDAT frame_data(i*8+4 to i*8+7);
}

if (cpu_read PORT::no::MISCSTAT & 0x180)
  cpu_write PORT::no::MISCFIFO 2; /* Discard injected data */
else
  cpu_write PORT::no::MISCFIFO 1; /* Send frame */
```

The advantage of the first method is that the routine only has to be run once when a frame is transmitted. The disadvantage is that it takes much longer to run, when transmit rate is an issue. The cpu_read required in each eight-byte cycle takes more than 0.4 µs, whereas each write only takes approximately 40 ns on the parallel interface.

The second method is much faster, but it must be run more than once if the data has to be discarded at the final check. Which method is better depends on the application.

3.10 MII Management Bus

Two MII Management controllers exist for accessing PHY registers. They are accessed as controller 0 and controller 1 through the register interface, each with a set of registers configuring rate of the MDC clock, action to perform, and so forth. Controller 0 is attached to the internal PHYs, and therefore only reacts on addresses 0-4 (for more information, see "Port Numbering," page 37). Controller 1 is attached to the MDC and MDIO pins of SparX-G5e. The rate of MDC for both controllers can be configured in the range from 1.2 MHz to 78 MHz. For more information about configuring the rate for MDC, see the PRESCALE_VALUE bit in "MII-M Prescaler—MIIMPRES (Address 0x03)," page 176. For more information about the specifications for MDC, see "AC Specifications for MII Management," page 233. For speeding up the access time, it is possible to run the interface without MDIO preamble – which is IEEE-optional.

The controllers are programmed with target PHY address, register index, and write data. A status register indicates when the operation is complete.

The operation is set up in the MIIMCMD register, status is read from the MIIMSTAT register, and the read result can be found in the MIIMDATA register.

The two controllers are selected by using either subblock 0 or subblock 1.

3.10.1 Scan Operation

The controllers also have the ability to scan a range of PHYs, mainly for automatic polling of link status from the PHYs' status registers. The scan feature is programmed with:

- The range of PHY addresses to be read.
- The index of the register to be read from each PHY.
- A value mask (PHY_REG_MASK) used to mask out the bits that are to be checked.

SparX-G5e continuously reads the specified register bits in the PHYs within the specified PHY range. When the register value is available, a scan result register (MIIMSRES) has the bit position corresponding to the PHY address read updated. This bit value is set to 1 if all the bits set in the value mask are also set in the read reply.

To handle multiple changes in the response from a PHY between two CPU reads of the MIIMSRES register, only the first change in each PHY's scan result is saved, until the CPU has read the result register.

The following is an example of how to continuously update the Link Status for PHY numbers 10 through 17.

- Set MIIMSCAN to PHY_ADDR_LOW = 10, PHY_ADDR_HIGH = 17, and PHY_REG_MASK = 0x0004.
- Set MIIMCMD to SCAN, READ, PHY_ADDR = 10, and PHY_REG = 1.

Bit 10-17 in the MIIMSRES register now reflects the link status of PHYs 10 through 17.

In the above example, it is assumed that the link status of the PHYs is found in register 1, bit 2 (the common position in most PHYs).

3.11 Counters

SparX-G5e has a flexible counter system that allows collection of any counter defined in the RMON statistics group (RFC2819, RFC2021). The octet counters are 32 bits wide, whereas frame counters are 24 bits wide. This guarantees that no counter wraps in less than 10 seconds.

SparX-G5e can simultaneously monitor three configurable frame events for Rx and three for Tx on a per-port basis. In addition, both an Rx and a Tx octet counter are present.

The Rx and Tx frame counters are configured per port in the CNT_CTRL_CFG register, which holds information about what event the Rx and Tx counters must monitor and count. The frame counter values are read in C_RX0, C_RX1, C_RX2, C_TX0, C_TX1, and C_TX2, whereas the octet counters are read in C_RXOCT and C_TXOCT. The counters are reset per port by writing any value to C_RX0.

The counters are by default set up to count the following events:

- C_RX0: packets received
- C_RX1: broadcasts + multicasts
- C_RX2: error packets
- C_TX0: packets transmitted
- C_TX1: broadcasts + multicasts
- C_TX2: error packets

The next section describes how the RMON statistics group (RFC 2819, RFC2021), the IEEE Std 802.3-2002 Annex 30A counters, and the SNMP interfaces Group MIB (RFC 1213 and 1573) map to a counter setup.

The numbers in parentheses in the following tables indicate the value that must be written to CNT_CTRL_CFG to set up a counter to monitor the desired event.

3.11.1 RMON Statistics Group (RFC 2819)

Table 20. Mapping of RMON Ethernet Statistics (RFC 2819 and 2021)

RMON Counter	RX/TX	CNT_CTRL_CFG Setup / Counter Register
EtherStatsDropEvents	RX	FIFO drops (13)
EtherStatsOctets	RX	Rx Octets/C_RXOCT
EtherStatsPkts	RX	Packets (0)
EtherStatsBroadcastPkts	RX	Broadcasts (3)
EtherStatsMulticastPkts	RX	Multicasts (4)
EtherStatsCRCAlignErrors	RX	CRC (16)
EtherStatsUndersizePkts	RX	Undersize (17)
EtherStatsOversizePkts	RX	Oversize (18)
EtherStatsFragments	RX	Fragments (19)
EtherStatsJabbers	RX	Jabbers (20)
EtherStatsPkts64Octets	RX	64 (5)
EtherStatsPkts65to127Octets	RX	65 (6)

Table 20. Mapping of RMON Ethernet Statistics (RFC 2819 and 2021) *(continued)*

RMON Counter	RX/TX	CNT_CTRL_CFG Setup / Counter Register
EtherStatsPkts128to255Octets	RX	128 (7)
EtherStatsPkts256to511Octets	RX	256 (8)
EtherStatsPkts512to1023Octets	RX	512 (9)
EtherStatsPkts1024to1518Octets	RX	1024 (10)
EtherStatsDroppedFrames (RMON-II)	RX	Never triggered – always zero
EtherStatsDropEvents	TX	FIFO drops (13) + Drops (14)
EtherStatsOctets	TX	Tx Octets/C_TXOCT
EtherStatsPkts	TX	Packets (0)
EtherStatsBroadcastPkts	TX	Broadcasts (3)
EtherStatsMulticastPkts	TX	Multicasts (4)
EtherStatsCollisions	TX	Collisions (15)
EtherStatsPkts64Octets	TX	64 (5)
EtherStatsPkts65to127Octets	TX	65 (6)
EtherStatsPkts128to255Octets	TX	128 (7)
EtherStatsPkts256to511Octets	TX	256 (8)
EtherStatsPkts512to1023Octets	TX	512 (9)
EtherStatsPkts1024to1518Octets	TX	1024 (10)
EtherStatsDroppedFrames (RMON-II)	TX	Never triggered – always zero

3.11.2 Ethernet MIB (IEEE Std 802.3-2002 Annex 30A Counters)

Only counter groups with supported counters are shown in the following tables.

Table 21. Mandatory Counters

Counter	RX/TX	Implementation in SparX-G5e
aFramesTransmittedOK	TX	Packets (0).
aSingleCollisionFrames	TX	N/A.
aMultipleCollisionFrames	TX	N/A.
aFramesReceivedOK	RX	Total good packets (25).
aFrameCheckSequenceErrors	RX	N/A. CRC (16) is the sum of FCS errors and Alignments errors.
aAlignmentErrors	RX	N/A. CRC (16) is the sum of FCS errors and Alignments errors.

Table 22. Optional Counters

Counter	RX/TX	Implementation in SparX-G5e
aMulticastFramesXmittedOK	TX	Multicasts (4)
aBroadcastFramesXmittedOK	TX	Broadcasts (3)
aMulticastFramesReceivedOK	RX	Multicasts (4)
aBroadcastFramesReceivedOK	RX	Broadcasts (3)
aInRangeLengthErrors	RX	N/A
aOutOfRangeLengthField	RX	N/A
aFrameTooLongErrors	RX	Oversize (18)

Table 23. MAC Control Recommended Counters

Counter	RX/TX	Implementation in SparX-G5e
aMACControlFramesTransmitted	TX	N/A
aMACControlFramesReceived	RX	Control packets (21)
aUnsupportedOpcodesReceived	RX	N/A

Table 24. Pause MAC Control Recommended Counters

Counter	RX/TX	Implementation in SparX-G5e
aPauseMACControlFramesTransmitted	TX	Pause (12)
aPauseMACControlFramesReceived	RX	Pause (12)

3.11.3 Mapping of SNMP Interface Group MIB – MIB-II (RFC 1213 and 1573)

Table 25. SNMP Counters in RFC 1213 and 1573

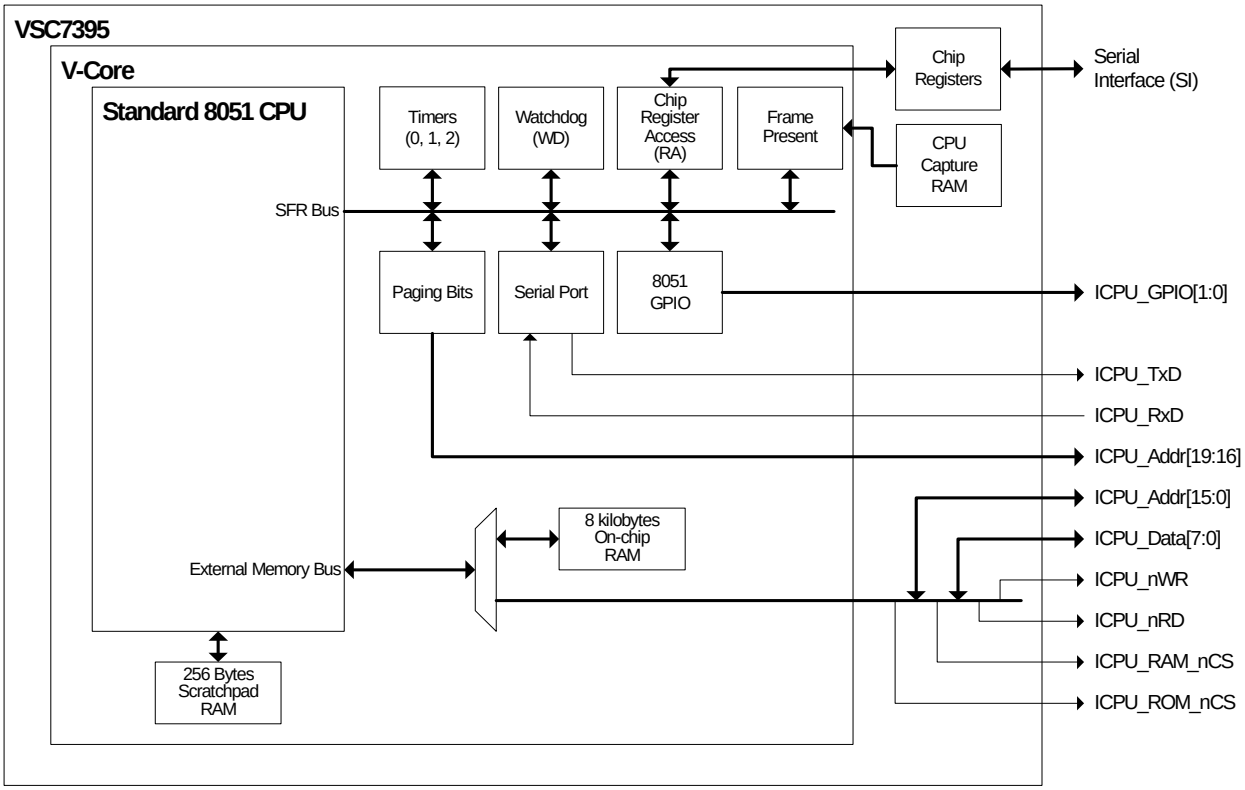
Counter	RX/TX	Implementation in SparX-G5e
ifInOctets	RX	Rx Octets/C_RXOCT
ifInUcastPkts	RX	Total good packets (25) – Broadcasts + Multicasts (1)
ifInNUcastPkts	RX	Broadcasts + Multicasts (1)
ifInBroadcast (RFC 1573)	RX	Broadcasts (3)
ifInMulticast (RFC 1573)	RX	Multicasts (4)
ifInDiscards	RX	FIFO drops (13) + Classifier drops (15)
ifInErrors	RX	Total error packets (2)
ifInUnknownProtos	RX	N/A
ifOutOctets	TX	Tx Octets/C_TXOCT
ifOutUcastPkts	TX	Total good packets (0) – Broadcasts + Multicasts (1)
ifOutNUcastPkts	TX	Broadcasts + Multicasts (1)
ifOutMulticast (RFC 1573)	TX	Multicasts (4)
ifOutBroadcast (RFC 1573)	TX	Broadcast (3)
ifOutDiscards	TX	FIFO drops (13) + Drops (14)
ifOutErrors	TX	Total error packets (2)

4 V-Core CPU

This section describes the additional features of the VSC7395 V-Core CPU (an integrated 8051) as compared to a standard 8051 CPU. For more information about the original 8051 characteristics, see the datasheet or user's manual of a standard 8051 implementation.

The following figure provides an overview of the V-Core CPU with its additional features and interfaces to its surroundings.

Figure 21. V-Core CPU Block Diagram



The V-Core CPU is designed to replace the functionality of an external CPU, effectively eliminating the necessity of external computational aids. Only a preprogrammed external flash memory or a serial bootprom is needed for booting up the V-Core CPU.

Two strapping pins, ICPU_PI_En and ICPU_SI_Boot_En, are used to configure the V-Core CPU.

The ICPU_PI_En pin selects the ownership of the parallel interface (PI) of the device.

- If ICPU_PI_En is strapped low, the V-Core CPU does not have access to the PI, and the PI functions as the regular parallel interface. For more information about the regular parallel interface, see "Parallel Interface," page 135.
- If ICPU_PI_En is strapped high, the V-Core CPU is able to access external flash and RAM through the interface. If, at the same time, ICPU_SI_Boot_En is strapped low, the V-Core CPU boots from this interface.

For clarity, the parallel interface pins are named according to their function with respect to the V-Core CPU. For a mapping table that shows the relationship between the logical pin names listed on the right side of the V-Core CPU block diagram shown previously and the real pin names, see Table 27, page 103. This is to avoid pin name confusion as a result of the shared use of the V-Core CPU's RAM/ROM interface and SparX-G5e's parallel interface.

When the other strapping pin, ICPU_SI_Boot_En, is strapped high, a hardware bootstrapper copies the contents of an external EEPROM attached to the serial interface into the 8-kilobyte on-chip RAM. When the copying is complete, the bootstrapper maps the on-chip RAM into address 0, releases the V-Core CPU from reset, and returns the serial interface to its normal function.

When both ICPU_SI_Boot_En and ICPU_PI_En are strapped low, the V-Core CPU is initially kept reset. However, an external CPU may load a program into the on-chip RAM and release the V-Core CPU from reset.

The following table summarizes these modes.

Table 26. Configurations for ICPU_SI_Boot_En and ICPU_PI_En

Configuration	ICPU_SI_Boot_En	ICPU_PI_En
V-Core CPU is enabled and boots from the SI and subsequently has access to PI.	Pull high	Pull high
V-Core CPU is enabled and boots from the SI, but does not subsequently have access to the PI.	Pull high	Pull low
V-Core CPU is initially disabled, but an external CPU may load an image into the on-chip RAM and enable the V-Core CPU.	Pull low	Pull low
V-Core CPU is enabled and boots from the PI.	Pull low	Pull high

The boot processes and interface protocols and associated registers are described in subsequent sections. The registers are divided into two groups: SFRs (Special Function Registers) and chip registers. Chip registers may be accessed by both an external CPU connected to the serial interface and by the V-Core CPU, whereas SFRs are accessible only by the V-Core CPU using MOV instructions. To distinguish between the two register varieties, SFR:: is used as a prefix with the SFR and CHIP:: is used with the chip registers. For more information about these registers, see "Registers," page 129.

4.1 Organization

The 8051 CPU has separate address spaces for program and data memory. In the V-Core CPU, program memory is accessible only through the external memory bus (for more information, see Figure 21). By default, eight kilobytes of on-chip RAM overlay the upper eight kilobytes of the 64-kilobyte address space, when ICPU_PI_En is strapped high. When ICPU_PI_En is strapped low, the on-chip RAM is repeated throughout the address space. The V-Core CPU fetches instructions only from the external memory bus. The same bus is used for external data memory accesses (MOVX instructions). Instruction fetches and external data accesses do not occur simultaneously, which makes it possible to share the address and data buses for such accesses. To distinguish between the different accesses, the V-Core CPU provides different control signals, which are explained in the following sections. By default, the on-chip RAM is mapped into the data space the same way as it is mapped into external program memory space.

In addition to the external memory bus, the V-Core CPU incorporates an internal memory bus, which is used to access the scratchpad RAM.

4.1.1 Scratchpad RAM

The scratchpad RAM is located in the internal data space, which is 256 bytes deep and is accessed through MOV instructions.

In many standard 8051 datasheets, the scratchpad RAM is known as the internal data memory. To distinguish this from the eight kilobytes of on-chip RAM, the term scratchpad RAM is used for the 256 bytes of RAM accessed through MOV instructions.

The scratchpad RAM on the V-Core CPU is 256 bytes, whereas it is 128 bytes on a standard 8051 implementation.

Direct accesses to addresses greater than 0x7F end up on the SFR bus. The additional 128 bytes of scratchpad RAM may only be referenced by indirect addressing. Indirect addressing always refers to the scratchpad RAM, never to an SFR.

Therefore, to read the value contained at the internal RAM address 0x98, the developer may write code similar to the following:

```
MOV R0, #0x98; Set the indirect address to 0x98
MOV A,  @R0  ; Read the contents of the scratchpad RAM
             ; pointed to by R0
```

However, when accessing the SFR directly, the developer may write the following code:

```
MOV A, 0x98  ; Reads the contents of SFR 0x98 (SCON)
```

which reads the value of SFR 0x98, which is the SCON register.

The upper 128 bytes of the scratchpad RAM is not bit-accessible but may be used as stack space, for example.

4.1.2 Paging

Paging is only available if ICPU_PI_En is strapped high. If ICPU_PI_En is strapped low, writing to the page registers that are described in the following has no effect.

Before describing the external memory layout, it is necessary to have a basic understanding of the paging mechanism. Fundamentally, the 8051 is only able to access 64 kilobytes of external data or program memory because its address bus is only 16 bits wide. The paging mechanism extends the width of the address bus by four bits. These four bits end up on the ICPU_Addr[19:16] pins. By connecting these pins to the most significant address bits of an external Flash or external RAM, the total memory space is extended up to 1 megabyte.

Because the V-Core CPU only holds instructions to access 64 kilobytes of memory, the page bits must be set programmatically. The PG SFR is intended for this purpose. This SFR contains two groups of four bits each: IFP[3:0] and OP[3:0]. The IFP group holds the four page bits used for instruction fetches and programmatic program memory reads (MOVC instructions), whereas the OP group holds the four page bits used for all other types of external memory accesses, that is, program memory writes, data memory reads, and data memory writes (not program memory reads).

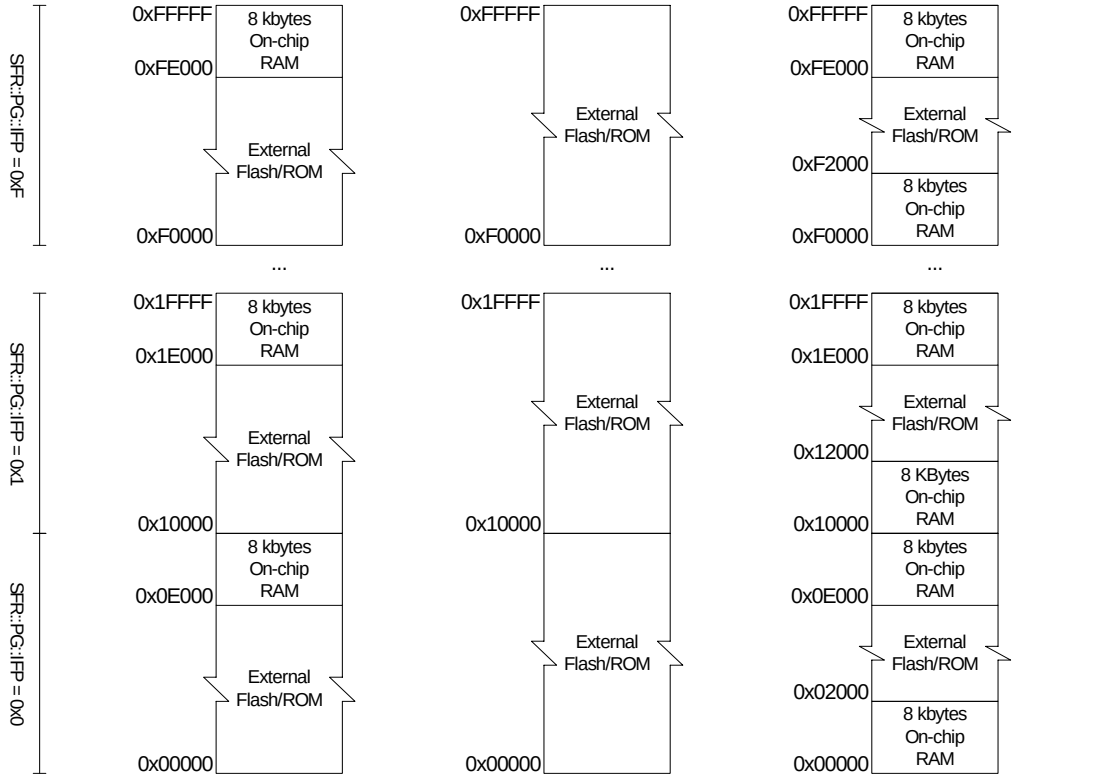
By dividing the page bits into two chunks, the V-Core CPU may, for instance, execute code from different pages of the Flash while reading data from a separately numbered RAM page. The PG SFR is located on an address divisible by eight, which makes it bit-addressable (read-modify-write).

4.1.3 External Program Memory

This section only applies if ICPU_PI_En is strapped high. If ICPU_PI_En is strapped low, the on-chip RAM is repeated throughout the address space, and writes to the mapping registers described below are ignored.

When reset, the V-Core CPU begins execution of code from address 0x0000. This location is mapped by default to external Flash or ROM as shown in the power-on configuration example (a) in the following figure. This figure provides three program memory layout examples for program memory reads with ICPU_PI_En strapped high.

Figure 22. Layout Examples for Program Memory Reads with ICPU_PI_En Strapped High



a. Example of power-on configuration:
ICPU_PI_En strapped high
CHIP::SYSTEM::ICPU_ROM_MAP::MAP_7=1
CHIP::SYSTEM::ICPU_ROM_MAP::MAP_6-0=0
(CHIP::SYSTEM::ICPU_CTRL::BOOT_EN=0)

b. Example of on-chip RAM disabled in all regions
ICPU_PI_En strapped high
CHIP::SYSTEM::ICPU_ROM_MAP::MAP_*=0
(CHIP::SYSTEM::ICPU_CTRL::BOOT_EN=0)

c. Example of on-chip RAM enabled in boot area:
ICPU_PI_En strapped high
CHIP::SYSTEM::ICPU_ROM_MAP::MAP_7-1=0
CHIP::SYSTEM::ICPU_ROM_MAP::MAP_0=1
(CHIP::SYSTEM::ICPU_CTRL::BOOT_EN=1)

It is important to note that this figure only shows the memory layout for program memory *reads* (both instruction fetches and programmatic reads using MOVC instructions). All program memory writes are forwarded to the external interface. Consequently, the code can execute in the on-chip RAM while programming the Flash addresses that it overlays.

With the SparX-G5e device in the power-on configuration, the upper eight kilobytes of each 64-kilobyte segment are overlaid with the on-chip RAM for program memory reads. This means that all instruction fetches in this area are forwarded to the on-chip RAM rather than to the external Flash. The left side of the previous figure shows how the value of the IFP page bits affects the addresses accessed, and that the on-chip RAM is repeated throughout the 1 megabyte of address space. The OP page bits take effect when *writing* to program memory.

The CHIP::SYSTEM::ICPU_ROM_MAP register controls the mapping of the on-chip RAM in the 64-kilobyte program memory space. The register contains eight bits (MAP_x), one for each eight-kilobyte region. For example, when MAP_7 is set, the on-chip RAM is mapped into the program memory at addresses 0xE000 through 0xFFFF (in all pages). When MAP_0 is set, the on-chip RAM is mapped into program memory on addresses 0x0000 through 0x1FFF. Zero or more bits may be set as desired. Therefore, if all eight bits are set the on-chip RAM is repeated throughout the address space.

The example (b) of the on-chip RAM disabled in all regions shows the situation where all ICPU_ROM_MAP::MAP_x bits are cleared, that is, where the on-chip RAM does not overlay any of the program memory addresses. For more information about example (b), see Figure 22, page 99.

SYSTEM::ICPU_ROM_MAP::MAP_0 is mirrored in the SYSTEM::ICPU_CTRL::BOOT_EN bit. This feature is very useful in conjunction with the SOFT_RST bit in the ICPU_CTRL register.

If, for example, the V-Core CPU is currently executing from the lower eight-kilobytes of Flash and the Flash needs to be reprogrammed, boot code can be copied from the Flash into the on-chip RAM prior to booting from the on-chip RAM. The V-Core CPU now writes to the ICPU_CTRL register with both SOFT_RST and BOOT_EN set, effectively causing the on-chip RAM to be mapped in before the boot commences from it. This situation is shown in example (c); for more information, see Figure 22, page 99. This situation is very similar to the one that appears after boot when ICPU_SI_Boot_En is also strapped high.

Care should be taken not to toggle a MAP_x bit (and BOOT_EN) while executing code in the region controlled by that bit.

4.1.3.1 Writing to Program Memory Space

Contrary to the standard 8051 instruction set, the V-Core CPU includes functionality for writing to program memory space. The SPC_FNC SFR contains a bit, WRS, which, when set, causes writes to external memory to be made to flash rather than to RAM. WRS = 0 is the default, making writes compatible with a standard 8051. Therefore, a function to write to Flash may look like the following:

```
MOV  DPTR,    #0xABCD ; Load some address
MOV  A,       #0x12   ; Load some value
MOV  SPC_FNC, #1      ; Set WRS bit. Future writes are to Flash
MOVX @DPTR,   A       ; Write value to Flash
MOV  SPC_FNC, #0      ; Back to normal RAM accesses.
```

Even though all program memory writes are forwarded to the external interface independently of the setting of the ICPU_ROM_MAP::MAP_x bits, code can be loaded into the on-chip RAM by executing instructions on the V-Core CPU itself. The on-chip RAM is shared between program and data memory accesses. Therefore, by accessing the RAM as data, code can be copied into it. For more information, see "External Data Memory," page 101.

4.1.3.2 Reading and Executing Different Program Memory Pages

In many applications, the Flash is divided into a code page that holds the program to execute on the V-Core CPU and code pages that hold static data; for example, configuration. The problem now is to execute the code from the code page while programmatically reading the static data from the configuration pages. Normally, programmatic program memory reads are performed using MOVC instructions; however, because both instruction fetches and MOVC instructions use the same set of paging bits (SFR::PG::IFP), this is not possible.

The solution is to use the SPC_FNC2 SFR. This SFR contains one bit, ENA. When the ENA bit is set, all *data* accesses (both reads and writes, using MOVX instructions) are forwarded to Flash using the SFR::PG::OP bits.

In the following example, the V-Core CPU executes from Flash page #0 (that is, SFR::PG::IFP = 0x0), and reads one byte from address 0xABCD in page #1 of the Flash.

```
MOV  B,         PG       ; Save current paging bits
MOV  PG,        #1       ; Change OP to 1, leave IFP at 0
MOV  SPC_FNC2,  #1       ; Forward all MOVX accesses to Flash
MOV  DPTR,      #0xABCD  ; Load some address
MOVX A,         @DPTR    ; Read value from Flash page #1, offset 0xABCD
MOV  SPC_FNC2,  #0       ; Back to normal RAM accesses
MOV  PG,        B        ; Restore the paging bits
```

The V-Core CPU cannot access variables stored in external RAM while the SPC_FNC2::ENA bit is set. Therefore, it must have such variables stored either in the scratchpad RAM or in the on-chip RAM. In the latter case, the programmer must ensure that the on-chip RAM location is mapped into the *program* memory space using the SYSTEM::ICPU_ROM_MAP register. Be careful not to map it in at the same location as the program that is currently executing. The reason for mapping it using the ICPU_ROM_MAP, and not the ICPU_RAM_MAP, is that RAM accesses are unconditionally seen as ROM accesses as long as SPC_FNC2::ENA is 1.

When SPC_FNC2::ENA is set, the memory interface timing of MOVX instructions is dictated by the SYSTEM::ICPU_ROM_CFG register as expected, but the SFR::CKCON::MD settings dictate the width of the control signals. For more information, see "External Memory Interface and Timing Configuration," page 103.

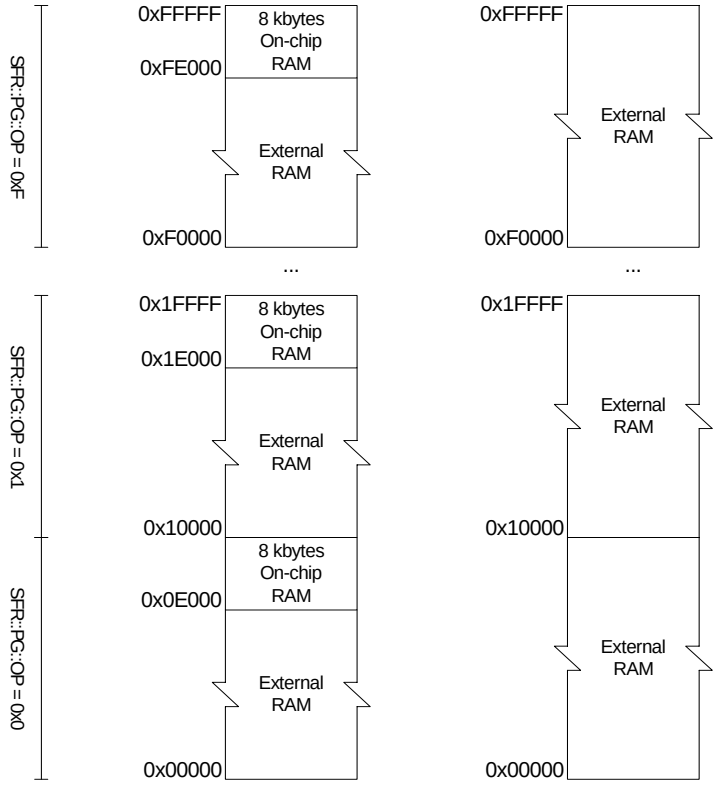
4.1.4 External Data Memory

This section only applies if ICPU_PI_En is strapped high. With ICPU_PI_En strapped low, the on-chip RAM is repeated throughout the address space, and writes to the mapping and paging registers have no effect.

Both read and write accesses to external data memory (MOVX instructions) use the same page bits, specifically SFR::PG::OP. In the power-up configuration, the on-chip RAM overlays the upper eight kilobytes of each page as shown in example (a) in Figure 23. Therefore, all reads and writes in this region are forwarded to the on-chip RAM rather than external RAM.

The MAP_x bits in the CHIP::SYSTEM::ICPU_RAM_MAP register control whether the on-chip RAM overlays particular regions. The following figure shows the on-chip RAM mapped out of the external data memory space in example (b), that is, all MAP_x bits are 0. In this situation, all RAM accesses are forwarded to the external RAM.

Figure 23. Two Data Memory Access Examples



a. Example with power-on configuration:
CHIP::SYSTEM::ICPU_RAM_MAP::MAP_7=1
CHIP::SYSTEM::ICPU_RAM_MAP::MAP_6-0=0

b. Example with on-chip RAM disabled in all regions:
CHIP::SYSTEM::ICPU_RAM_MAP::MAP_*=0

4.2 Pin Name Mapping

The following table shows the mapping from the logical V-Core CPU pin names used in this section to the pin names listed in "Pins by Name," page 263.

The interface is only effective if ICPU_PI_En is strapped high. However, the ICPU_RxD and ICPU_TxD pins are available in all configurations of the V-Core CPU.

Table 27. Pin Name Mapping Between the V-Core CPU and the Parallel Interface

Pin Name (V-Core CPU)	Pin Name (PI)	Pin Direction (V-Core CPU)	Pin Direction (PI)
ICPU_GPIO[1:0]	PI_IRQ[1:0]	I/O	O
ICPU_Addr[19:16]		O	
ICPU_Addr[15:0]	PI_Addr[15:0]	O	I
ICPU_Data[7:0]	PI_Data[7:0]	I/O	I/O
ICPU_nWR	PI_nWR	O	I
ICPU_nRD	PI_nOE	O	I
ICPU_RAM_nCS	PI_nDone	O	O
ICPU_ROM_nCS	PI_nCS	O	I
ICPU_TxD		O	
ICPU_RxD		I	

4.3 External Memory Interface and Timing Configuration

The external memory interface, which is active only if ICPU_PI_En is strapped high, is designed to attach most 8-bit RAMs and ROMs/Flashes. Because of the paging mechanism, up to 1 megabyte of each type of memory may be connected, but the V-Core CPU itself can only address 64 kilobytes.

The address and data buses (ICPU_Addr[19:16] and ICPU_Data[7:0]) are shared between RAM and ROM, which is possible because accesses occur in different time slots. The SparX-G5e device provides four control signals. Of these signals, ICPU_nWR and ICPU_nRD control whether a read or a write access is in progress. These signals are active low and should be connected to both RAMs and ROMs.

Two other control signals, ICPU_RAM_nCS and ICPU_ROM_nCS, determine whether a RAM or ROM access, respectively, is in progress. These signals are also active low and should be connected to RAMs and ROMs, respectively.

The interface is highly configurable enabling support of both RAMs and Flashes that latch data on the falling edge or the rising edge of either the write or chip-select signal. Therefore, the SparX-G5e device implements configuration registers for configuring both the displacement and the width of the control signals (ICPU_nRD, ICPU_nWR, ICPU_RAM_nCS, and ICPU_ROM_nCS).

For more information about read and write timing diagrams for RAM and Flash accesses, see "Electrical Specifications," page 217.

4.3.1 Control Signal Width Configuration

The width of the control signals is determined by two parameters:

- The internal clock frequency of the V-Core CPU. At power-on, this is set to 1/32 of the system clock frequency corresponding to 204.8 ns per clock cycle. The clock period can be controlled through the CLK_DIV field in the CHIP::SYSTEM::ICPU_CTRL register and should never be set lower than the external memories can handle.
- The value of the SFR::CKCON::MD[2:0] bits. The following table shows the width of the control signals as a function of these three bits.

Table 28. Control Signal Width as a Function of the CKCON::MD2-0 SFR Value

MD[2:0]	Control Signal Width in V-Core CPU Clock Cycles
0	2
1	4 (default)
2	8
3	12
4	16
5	20
6	24
7	28

The value of the MD[2:0] bits controls all RAM accesses and Flash writes. Flash reads are not affected by the value of these bits. However, the V-Core CPU clock frequency still affects the width of flash reads, which is always two V-Core CPU clock cycles.

4.3.2 Control Signal Displacement Configuration

Two chip registers, CHIP::SYSTEM::ICPU_RAM_CFG and CHIP::SYSTEM::ICPU_ROM_CFG, control the displacement of the control signals. Reads and writes are controlled individually, as described in the following sections.

4.3.2.1 RAM Reads

When the V-Core CPU reads from external RAM, the parameters configured in the ICPU_RAM_CFG register govern. The register contains two fields, CHIP_SEL_READ_DELAY and READ_DELAY, which control how the ICPU_RAM_nCS and ICPU_nRD signals, respectively, are displaced with respect to the address. Each of the two signals can be displaced up to 44.8 ns in steps of 6.4 ns.

4.3.2.2 RAM Writes

Control signal displacement of write accesses to external RAM is configured through the CHIP_SEL_WRITE_DELAY and WRITE_DELAY fields of the ICPU_RAM_CFG register. As for reads, the two signals can be displaced up to 44.8 ns in steps of 6.4 ns.

In addition, the V-Core CPU can be configured to hold the written data (ICPU_Data) up to 44.8 ns longer than normal. This is controlled through the WRITE_DATA_HOLD field of the register.

4.3.2.3 ROM/Flash Reads

The displacement of control signals for ROM and Flash reads is configured through the CHIP_SEL_READ_DELAY and READ_DELAY fields of the ICPU_ROM_CFG register. The displacement can be up to 44.8 ns (the default is 6.4 ns, which allows most 8-bit Flashes to work with SparX-G5e during boot-up).

4.3.2.4 Flash Writes

Writes to an external flash are controlled through the CHIP_SEL_WRITE_DELAY and WRITE_DELAY fields of the ICPU_ROM_CFG register. The displacement can be up to 44.8 ns.

In addition, the V-Core CPU can be configured to hold the written data (ICPU_Data) up to 44.8 ns longer than normal. This is controlled through the WRITE_DATA_HOLD field of the register.

4.3.3 Power-On and Reset Timing

After power-on-reset, the clock period of the V-Core CPU is set to 1/32 of the system clock period, or 204.8 ns. The first instruction fetch from the Flash's address 0x0000 occurs approximately six V-Core CPU clock cycles (1228 ns) after the release of the chip's nReset signal.

4.4 SI EEPROM Booting

Booting the V-Core CPU from an external, serial EEPROM attached to the serial interface is enabled when ICPU_SI_Boot_En is strapped high. Upon a chip reset, the hardware boot strapper copies the program image from the EEPROM to the on-chip RAM of the V-Core CPU, and releases the V-Core CPU from reset. This is sufficient for unmanaged applications.

The software image can have a maximum size of eight kilobytes and must comply with the following format:

- The two first bytes indicate the number of bytes in the image including the one-byte checksum, but excluding the length.
- The last byte of the image is a checksum byte. Adding all bytes in the image – including the checksum byte, but excluding the length bytes – must equal 0.
- The byte format of the image data must be big endian.

The protocol for booting from the EEPROM is as follows:

1. The feature is enabled by strapping ICPU_SI_Boot_En high.
2. When releasing nReset, SparX-G5e starts generating the SI_Clk after 10-20 ms. The SI_Clk frequency is 200 KHz.
3. Immediately after step 2, SparX-G5e initiates a read sequence starting from address 0. SI_nEn is kept low until the entire image is read. The size of the image is given by the first two bytes read.
4. The boot strapper writes the EEPROM image into the V-Core CPU's internal eight-kilobyte RAM starting from address 0. During booting, the V-Core CPU is held reset.
5. After booting (checksum is correct), the boot strapper sets ICPU_ROM_MAP::MAP_0, thereby instructing the V-Core CPU to execute from internal RAM instead of external RAM. Finally, the boot strapper releases the V-Core CPU reset, and the V-Core CPU executes from the loaded image.

Where there is an incorrect checksum, the V-Core CPU is still released from reset. To indicate the error condition, the SI_Do pin goes high for approximately 4 µs to 5 µs. Additionally, the error condition is indicated in SYSTEM::SIMASTER::CHKSUM_ERR.

If ICPU_PI_En is also strapped high, the V-Core CPU has access to external RAM/Flash through the PI after the SI boot completes.

For more information about the SI read operation sequence when booting from an EEPROM, see Figure 31, page 135.

4.5 Clock Frequency Select

The V-Core CPU runs in its own clock domain and can be programmed to run at frequencies ranging from approximately 4.9 MHz to 78.1 MHz. Because the V-Core CPU clock frequency directly reflects the timing on the external RAM/ROM interface, the slowest possible frequency is chosen after a power-on reset, that is, 4.9 MHz or 204.8 ns per clock period.

The frequency is controlled from the CLK_DIV field in the CHIP::SYSTEM::ICPU_CTRL register and is computed using the formula:

$$F_{iCPU} = \frac{156.25}{CLK\_DIV + 1} MHz, CLK\_DIV \in [1;31]$$

After selecting an external Flash and RAM, the frequency can be trimmed to match the access time of the external memory. This new frequency needs to be programmed by the V-Core CPU code after boot-up.

In configurations where ICPU_PI_En is strapped low, the highest possible frequency can be selected, because the V-Core CPU only executes from on-chip RAM.

4.6 Reset Options

The chip can be programmatically reset (soft reset) in three different ways:

- Reset the chip including the V-Core CPU.
- Reset the chip excluding the V-Core CPU.
- Reset only the V-Core CPU.

4.6.1 Reset Chip Including the V-Core CPU

Resetting the whole chip corresponds very closely to a power-on reset and causes all registers to return to their default values. This means that the whole chip needs to be re-initialized from the very beginning after such a reset using the initialization sequence guidelines. For more information, see "Initialization Sequence," page 140.

The reset is carried out by first performing a write to the CHIP::SYSTEM::GLORESET register with the STROBE field set and the remaining fields cleared. This is followed by a write to the same register but this time with the MASTER_RESET field set and the remaining fields cleared.

Note If both ICPU_PI_En and ICPU_SI_Boot_En are strapped low, the V-Core CPU requires assistance from an external CPU to get out of reset again. For more information, see "External Access to On-Chip RAMs," page 118.

4.6.2 Reset Chip Excluding V-Core CPU

Omitting the V-Core CPU from a chip reset is sometimes desirable. The effect of such a reset is that all chip registers return to their default values, while the V-Core CPU register space (SFR) retains its values. One implication is that the programmed RAM or ROM displacement values (CHIP::SYSTEM::ICPU_RAM_CFG and CHIP::SYSTEM::ICPU_ROM_CFG) and the clock frequency configuration of the V-Core CPU are lost and need to be reprogrammed because these registers are located in the system domain.

Two different situations arise: If ICPU_PI_En is strapped low, the on-chip RAM will remain mapped into the whole address space, and there are no special concerns. If ICPU_PI_En is strapped high, care should be taken not to execute the resetting code from on-chip RAM when this is mapped to the lower eight kilobytes of code memory, that is, when CHIP::SYSTEM::ICPU_CTRL::BOOT_EN is set. This is because the reset clears the bit and therefore switches from executing from on-chip RAM to executing from external Flash/ROM. A safe method for keep executing the running program is to make sure that the actual reset procedure is carried out in the upper eight kilobytes of the 64 kilobytes memory space. During the chip reset, the program will continue to execute because the default value of SYSTEM::ICPU_ROM_MAP::MAP_7 is 1, which enables the on-chip RAM in the upper eight kilobytes of code memory. After the reset, set SYSTEM::ICPU_CTRL::BOOT_EN to 1 and jump back to the lower eight kilobytes. Interrupts should remain disabled throughout this operation.

The reset is carried out by first slowing the V-Core CPU to the slowest possible frequency (CHIP::SYSTEM::ICPU_CTRL::CLK_DIV=31), and then writing to the CHIP::SYSTEM::GLORESET register with both the ICPU_LOCK and STROBE bits set, leaving the remaining fields in the register cleared. This must be followed by a write to the same register, this time with MASTER_RESET set and the remaining fields cleared. The last chip register write must be followed by a write to the SFR::RA_DONE with the DONE bit set to clear the hardware state machine; for more information, see "Chip Register Writes," page 110. The chip must be re-initialized by following the initialization sequence guidelines. For more information, see "Initialization Sequence," page 140.

4.6.3 Reset V-Core CPU Only

The last type of reset is where only the V-Core CPU is reset; the rest of the chip keeps running unaffected. All chip registers retain their values, whereas the SFRs are reset to default. Consequently, when the V-Core CPU starts up again, it keeps running at the previously programmed frequency, and the external memories' access configuration is also the same.

To invoke such a reset, first write to the CHIP::SYSTEM::SYSTEM_GLORESET register with the MEM_LOCK and STROBE bit set and the remaining fields cleared. Then write to the CHIP::SYSTEM::ICPU_CTRL register with the SOFT_RST bit cleared. This causes an immediate reset of the V-Core CPU.

If either of the ICPU_PI_En and ICPU_SI_Boot_En pins are strapped high, the SOFT_RST bit is auto-set by hardware when the reset is over. If both strapping pins are strapped low, the SOFT_RST bit will not be cleared after reset, and an external CPU's assistance is needed in order to have the V-Core CPU out of reset (for more information, see "External Access to On-Chip RAMs," page 118.

This kind of reset is useful, for example, when the on-chip RAM is loaded with boot code and the user wants to boot from it. Instead of just setting the SOFT_RST bit in the CHIP::SYSTEM::ICPU_CTRL register, the user also sets the BOOT_EN bit. This causes the on-chip RAM to be mapped to address 0x0000 of the program memory space, effectively causing the boot to happen from the on-chip RAM.

The V-Core CPU may be kept reset using the CHIP::SYSTEM::ICPU_CTRL register's SOFT_RST_HOLD bit. To enable this feature, set SOFT_RST_HOLD to 1 while clearing the SOFT_RST bit. After such an operation, assistance is needed from the external CPU to get the V-Core CPU out of the reset state.

4.7 Interrupts

The V-Core CPU supports six interrupt sources: two external interrupts, three timer interrupts, and the serial port interrupt.

The IE and IP SFRs provide interrupt enable and priority control, as with a standard 8051. The IE::EA bit (Enable All) is a global enable for all interrupts. When IE::EA is 1, each interrupt is enabled or masked by its individual enable bit in the IE register.

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt. The vector address is shown in the interrupt vector column of Table 29. The V-Core CPU always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI or a write access to any of the IP or IE SFRs, the V-Core CPU completes one additional instruction before servicing the interrupt.

The interrupt latency depends on the current state of the V-Core CPU. The fastest response time is five instruction cycles; one to detect the interrupt and four to perform the LCALL to the ISR. This is equivalent to 20 V-Core CPU clock cycles. The maximum latency occurs when the V-Core CPU is currently executing a RETI instruction followed by a MUL or DIV instruction. The 13 instruction cycles (52 clock cycles) in this case are: one to detect the interrupt, three to complete the RETI, five to execute the DIV or MUL, and four to execute the LCALL to the ISR.

Each ISR ends with a RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An interrupt can only be interrupted by a higher-priority interrupt. The interrupts listed in Table 29 are organized in decreasing natural interrupt priority. In addition to the natural priority, an interrupt can be assigned a high-priority level or low-priority level, which takes precedence over the natural priority. This selection is made with the IP SFR. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. After an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

The two so-called external interrupts—External Interrupt #0 and #1—are connected to the FP (Frame Present) module and to the GPIO module, respectively. For more information about the Frame Present module, see "Frame Present Module," page 112. In a standard 8051, these two interrupts are active low. In the V-Core CPU implementation, they become active when either of the two SFR::FPSTAT::Qx bits transition from 0 to 1 and the corresponding SFR::FPIE::Qx is set (External Interrupt #0), or when the GPIO_IN::GI0 bit transitions from 0 to 1 (External Interrupt #1). When active, the IE::IEx ($x \in [0; 1]$) returns a 1.

These two interrupts can be programmed through the TCON::IT0 and TCON::IT1 bits to be either edge-sensitive or level-sensitive. For example, when TCON::IT0 is 0, the interrupt is level-sensitive and the V-Core CPU sets the TCON::IE0 flag when the logical AND of FPSTAT::Qx and FPIE::Qx samples high. When TCON::IT0 is 1, the interrupt is edge-sensitive and the V-Core CPU sets the TCON::IE0 flag when the logical AND of FPSTAT::Qx and FPIE::Qx samples low, then high on consecutive samples.

Table 29. Interrupts

Interrupt Name	Flags	Enable	Priority Control	Edge/Level Sensitivity	Interrupt Vector	Interrupt Number
External Interrupt #0	TCON::IE0 FPSTAT::Qx	IE::EX0 FPIE::Qx	IP::PX0	TCON::IT0	0x0003	0
Timer 0 Interrupt	TCON::TF0	IE::ET0	IP::PT0		0x000B	1
External Interrupt #1	TCON::IE1 GPIO_IN::GI0	IE::EX1	IP::PX1	TCON::IT1	0x0013	2
Timer 1 Interrupt	TCON::TF1	IE::ET1	IP::PT1		0x001B	3
Serial Port Tx or Rx Interrupt	SCON::TI SCON::RI	IE::ES	IP::PS		0x0023	4
Timer 2 Interrupt	T2CON::TF2	IE::ET2	IP::PT2		0x002B	5

4.8 Chip Register Access

The V-Core CPU uses indirect access to read and write the internal chip registers of the SparX-G5e device. The RA module located on the SFR bus interfaces between the V-Core CPU and the chip registers.

Chip registers are 32 bits wide and are addressed through a 3-bit block number, a 4-bit subblock number, and an 8-bit register address. The eight SFRs (RA_xxx) making up the RA module contain registers for holding this information before initiating a read or a write access. Accesses vary in execution time and a flag (SFR::RA_DONE::DONE) indicates when an access is complete. The following two sections explain write and read accesses.

4.8.1 Chip Register Writes

Four registers in the RA module are used to hold the 32-bit data value to write to the chip register. These four SFRs are named RA_DA0 through RA_DA3, with RA_DA0 designated to hold the least significant byte and RA_DA3 the most significant byte of the 32-bit value.

The RA_BLK register contains two fields, BLOCK and SUBBLOCK. The 3-bit block number and 4-bit subblock number of the register to access must be written to these fields.

Finally, write the register address within the block and subblock into SFR::RA_AD_WR. This operation initiates the real write access, effectively sending the data held in RA_DA0-3, RA_BLK, and RA_AD_WR to the chip register.

Only one chip register access can be in progress at a time. Because access time may vary from register to register, all write operations should enter a loop where they continuously poll the SFR::RA_DONE::DONE bit. As long as this bit is cleared, the write operation is still in progress and another access cannot be initiated. When the bit gets set, the write operation is complete, and the software must clear it by writing a 1 to it.

However, there is one situation where the DONE bit is never set by hardware, and that is when the V-Core CPU resets SparX-G5e without resetting itself. In this case, the DONE bit never gets set, but a 1 must still be written to it.

The following code sample writes 0x89ABCDEF to the chip register with block number 0x1, subblock number 0xA, and address 0x12.

```
        MOV RA_DA3,  #0x89; Bits[31:24] of data to write
        MOV RA_DA2,  #0xAB; Bits[23:16] of data to write
        MOV RA_DA1,  #0xCD; Bits[15: 8] of data to write
        MOV RA_DA0,  #0xEF; Bits[ 7: 0] of data to write
        MOV RA_BLK,  #0x2A; Write to block 0x1, subblock 0xA
        MOV RA_AD_WR,#0x12; Initiate write by specifying reg. address (0x12)
poll:   JNB RA_DONE, poll ; Wait for write to complete, i.e., DONE to get set
        MOV RA_DONE, #1   ; Prepare for next access by clearing DONE flag
```

The data written to the RA_DAx and RA_BLK registers is persistent. This implies that if the same value is written to several register addresses within the same block/subblock, new write-accesses can be initiated by simply writing a new value to the RA_AD_WR register followed by a poll of the DONE bit.

4.8.2 Chip Register Reads

Programming a read access is very much like programming a write access, except that the RA_DAx registers are read from rather than written to. As for the write access, fill in the RA_BLK with the block number and subblock number of the register to read, and initiate the *read* by *writing* the register address to RA_AD_RD. Poll the RA_DONE::DONE bit until it gets set and assemble the returned data by reading the RA_DAx SFRs. Reading the RA_DAx registers also clears the DONE flag.

The following code sample shows an example of a chip register read with block number 0x7, subblock number 0, and register address 0x10, which is the CHIP::SYSTEM::ICPU_CTRL register.

```
        MOV RA_BLK,  #0xE0 ; Read from block 0x7, subblock 0x0
        MOV RA_AD_RD,#0x10 ; Initiate read by specifying reg. address (0x10)
poll:   JNB RA_DONE, poll  ; Wait for read to complete,
                           ; that is, DONE bit to get set
        MOV R3,      RA_DA3; Bits[31:24] of returned data.
                           ; Also clears DONE bit
        MOV R2,      RA_DA2; Bits[23:16] of returned data.
        MOV R1,      RA_DA1; Bits[15: 8] of returned data.
        MOV R0,      RA_DA0; Bits[ 7: 0] of returned data.
```

The returned data remains in the RA_DAx registers until the next read completes. In fact, data written to the RA_DAx registers is different from the data returned by reading from the registers. Therefore, in the write function, it is not possible to verify the data just written to the registers because a read returns a different set of register values.

4.9 Frame Present Module

The V-Core CPU can extract frames from the CPU capture buffer. The two bits in CHIP::SYSTEM::CAPCTRL, QUEUE0_READY and QUEUE1_READY, indicate whether a capture queue contains frames. For more information about this process, see "Frame Capturing," page 85.

These two status bits are mirrored into the Q0 and Q1 bits of the FPSTAT SFR. This enables the V-Core CPU to perform faster polls of the queue status than if it had to read the chip register. An additional feature allows for interrupt-driven frame extraction. Another SFR, FPIE, contains two interrupt enable bits – one for each queue. Whenever interrupts are enabled for a particular queue and at least one frame is present in that queue, the External Interrupt #0 becomes active (provided IE::EX0 and IE::EA are also enabled). The FPIE::Qx bits operate independently from the corresponding Qx_IRQ_EN bits in the CHIP::SYSTEM::CAPCTRL register. This enables an external CPU connected to the SI interface to react on frames present in one queue, while the V-Core CPU handles frames from the other queue.

4.10 Watchdog

The Watchdog SFR module provides a means of preventing V-Core CPU software from running out of control. This is achieved by requiring that software periodically writes alternating values to the Watchdog after it is enabled. If it fails to do so within the Watchdog period, which is approximately 1.72 seconds, the Watchdog resets the V-Core CPU and sets a sticky bit in a chip register.

This bit, CHIP::SYSTEM::ICPU_CTRL::WATCHDOG_RST, can be tested by the V-Core CPU software during boot-up to see the reason for the boot. If it is 1, the Watchdog has reset it. If not, it was a normal boot. Write a 1 to the sticky-bit to clear it.

A reset caused by the Watchdog only involves the V-Core CPU; the rest of the chip is unaffected. This corresponds very closely to a V-Core CPU-reset; for more information, see "Reset V-Core CPU Only," page 108.

The Watchdog module implements two SFRs: one for enabling and disabling the Watchdog (WDCON) and another for keeping the Watchdog alive (WDDA).

To enable the Watchdog, write a 1 to SFR::WDCON::WD_EN. After it is enabled, software must alternately write the two values 0xBE and 0xEF to the WDDA register (the first being 0xBE) using a maximum of 1.72 seconds intervals. If software writes a value different from the expected, the Watchdog issues a reset immediately. After waking up from a reset, the Watchdog is always disabled, which prevents subsequent resets from occurring.

The Watchdog can be disabled at any time by clearing the SFR::WDCON::WD_EN bit. Disabling the Watchdog also resets the watchdog timer, so that a subsequent reactivation leaves software with 1.72 seconds before it needs to write to WDDA. It is strongly recommended that the Watchdog be disabled while programming the Flash.

4.11 Timer 2

The standard 8051 timers (Timer 0 and Timer 1) are 8-bit timers or counters only, whereas Timer 2 offers 16-bit capabilities. This makes Timer 2 suitable as baud rate generator for the serial port because it offers much better granularity for the baud rates (for more information, see "Serial Port," page 114).

The modes supported with Timer 2 are:

- 16-bit auto-reload timer or counter
- Baud rate generator

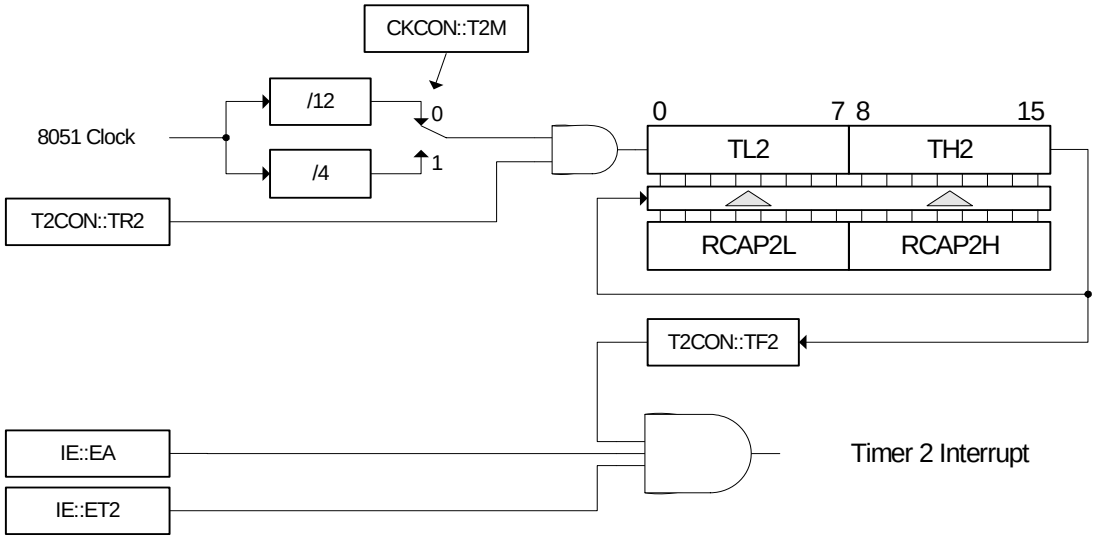
Timer 2 is an SFR module and is therefore configured using the SFR bus.

The default count-rate for all three timers is the same as for the standard 8051 timers, specifically 12 clock cycles per increment. This can be changed to 4 clock cycles per increment by setting the SFR::CKCON::TxM field to 1, where x is either 0, 1, or 2.

4.11.1 16-Bit Timer or Counter Mode with Auto-Reload

The following figure shows how Timer 2 operates in timer or counter mode with auto-reload. The T2CON::TR2 bit enables the counter. When it increments from 0xFFFF, the T2CON::TF2 flag is set, and the starting value is reloaded into TL2 and TH2 from RCAP2L and RCAP2H (which are programmed by software.) Upon overflow, an interrupt also occurs if the interrupt of Timer 2 is enabled (IE::ET2) and interrupts are globally enabled (IE::EA).

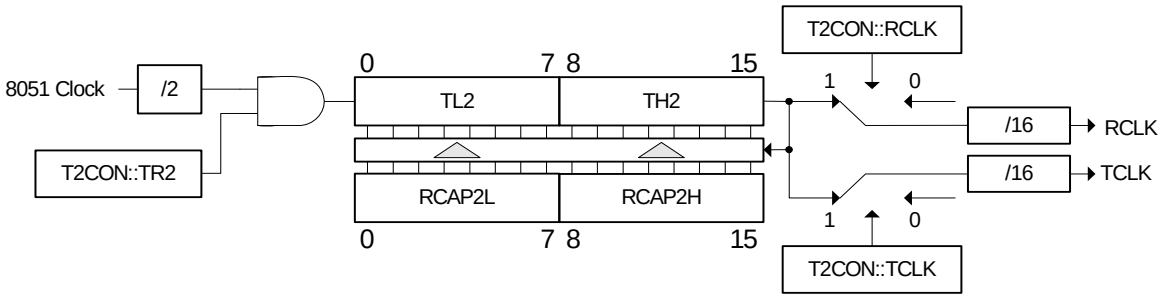
Figure 24. Timer 2 as Timer or Counter with Auto-Reload



4.11.2 Baud Rate Generator Mode

Setting either T2CON::RCLK or T2CON::TCLK to 1 configures Timer 2 to generate baud rates for the serial port in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow generates a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

Figure 25. Timer 2 as Baud Rate Generator



The counter time base in baud rate generator mode is calculated by dividing the 8051 clock by two.

4.12 Serial Port

The serial port provided in the V-Core CPU is identical in operation to the standard 8051 serial port. This section is provided to show how the serial port works with Timer 2, which is not part of the standard 8051 processor. The description is based in Mode 1 of the serial port. Mode 1 provides standard asynchronous, full-duplex communication using a total of ten bits: one start bit, eight data bits, no parity, and one stop bit (also known as 8N1). The serial port transmits on the ICPU_TxD pin and receives on the ICPU_RxD pin.

The baud rate is a function of timer overflow. The serial port can use either Timer 1 or Timer 2 as baud rate generator, but only Timer 2 is described in the following. Given a desired baud rate, *b*, the value to load into RCAP2L and RCAP2H of Timer 2 is computed as:

$$RCAP2H,RCAP2L = Round\left(65536 - \frac{f_{iCPU}}{32 \cdot b}\right)$$

where RCAP2H, RCAP2L is the value to write to RCAP2H and RCAP2L taken as a 16-bit unsigned integer, and f_{iCPU} is the V-Core CPU's current clock frequency. The 32 in the denominator is the result of the clock being divided by 2 and the Timer 2 overflow being divided by 16 (see Figure 25). The actual baud rate given an integral count can be computed as:

$$b = \frac{f_{iCPU}}{32 \cdot (65536 - RCAP2H, RCAP2L)}$$

Because it is the clock frequency of the V-Core CPU that forms the basis for the values to load into RCAP2x, it may be that not all baud rates are achievable with sufficient accuracy for all frequencies. The following table shows the deviation from the desired baud rate as a function of the V-Core CPU clock frequency for commonly used baud rates. As a rule of thumb, baud rates that cause deviations greater than 3% should be avoided.

Table 30. Baud Rate Deviations for Selected Clock Frequencies and Baud Rates

CLK_DIV (1)	f_{ICPU} [Hz]	Desired Baud Rate [bps]	RCAP2x	Actual Baud Rate [bps]	Deviation [%]
1	78,125,000	9,600	0xFF02	9,574.1	0.1
		115,200	0xFFEB	116,257.4	0.9
3	39,062,500	9,600	0xFF81	9,611.8	0.1
		115,200	0xFFF5	110,973.0	3.7
5	26,041,667	9,600	0xFFAB	9,674.4	0.3
		115,200	0xFFF9	116,257.4	0.9
6	22,321,429	9,600	0xFFB7	9,555.4	0.5
		115,200	0xFFFA	116,257.4	0.9
7	19,531,250	9,600	0xFFC0	9,536.7	0.7
		115,200	0xFFFB	122,070.3	6.0
8	17,361,111	9,600	0xFFC7	9,518.2	0.9
		115,200	0xFFFB	108,506.9	5.8
9	15,625,000	9,600	0xFFCD	9,574.1	0.3
		115,200	0xFFFC	122,070.3	6.0
10	14,204,546	9,600	0xFFD2	9,649.8	0.5
		115,200	0xFFFC	110,973.0	3.7
11	13,020,833	9,600	0xFFD6	9,688.1	0.9
		115,200	0xFFFC	101,725.3	11.7
12	12,019,231	9,600	0xFFD9	9,630.8	0.3
		115,200	0xFFFD	125,200.3	8.7
13	11,160,714	9,600	0xFFDC	9,688.1	0.9
		115,200	0xFFFD	116,257.4	0.9
17	8,680,556	9,600	0xFFE4	9,688.1	0.9
		115,200	0xFFFE	135,633.7	17.7
25	6,009,615	9,600	0xFFEC	9,390.0	2.2
		115,200	0xFFFE	93,900.2	18.5
31	4,882,813	9,600	0xFFF0	9,536.7	0.7
		115,200	0xFFFF	152,587.9	32.5

1. CLK_DIV refers to the value written to CHIP::SYSTEM::ICPU_CTRL::CLK_DIV.

The following code sample provides an example of a serial port initialization with the V-Core CPU running 4.9 MHz and a desired baud rate of 9600 bps. The serial port is configured to use Timer 2 and look up the value to write to RCAP2x and yields 0xFFEB.

```
MOV RCAP2H, #0xFF ; MSByte of baud rate divisor
MOV RCAP2L, #0xF0 ; LSByte of baud rate divisor
MOV T2CON,  #0x34 ; Use Timer 2 as baud rate generator
                  ; by activating both the RCLK, TCLK,
                  ; and the Timer 2 itself
MOV SCON,   #0x52 ; Set-up serial port to
                  ; Mode 1, REN=1 (receive enable)
MOV PS,     #0x1  ; Set high priority for Serial Port
                  ; interrupts (bit in IP SFR)
MOV ES,     #0x1  ; Enable serial port interrupt (bit in IE SFR)
MOV TH2,    #0xFF ; Force a new value into the counter, so that
                  ; the baudrate
MOV TL2,    #0xFF ; generation starts ASAP
```

The example also enables interrupt generation: transmit and receive interrupts. An interrupt handler must be installed to take care of this.

4.13 General-Purpose I/O

When ICPU_PI_En is strapped high, two pins on the SparX-G5e device are assigned to GPIO (ICPU_GPIO[1:0]) for the V-Core CPU. It is important not to confuse these pins with the device's GPIO pins, which are named GPIO[3:0]. With ICPU_PI_En strapped low, the dedicated V-Core GPIO is not present, and writes to the associated registers are ignored.

The V-Core CPU GPIO pins (referred to as GPIO in the following) are controlled from four SFRs: GPIO_IN, GPIO_OUT, GPIO_OE, and GPIO_STAT. The first three of these registers are located on SFR addresses divisible by 8, which make them bit addressable.

After reset, both pins are configured as inputs. The value currently found on an input pin is read from the GPIO_IN SFR. The pin directions are changed individually through the GPIO_OE, Output Enable, register. By setting a bit in this register, the corresponding GPIO pin is driven by the device with the value in the GPIO_OUT register.

The last of the four registers, GPIO_STAT, is used to track state changes in input values. If an input transitions from low to high or from high to low, the corresponding bit is set in GPIO_STAT. Software must write a 1 to the bit to clear it. When a pin is configured as output, the corresponding bit in GPIO_IN takes the value of the output. Therefore, changes in outputs also affect the value of the corresponding bits in GPIO_STAT.

ICPU_GPIO[0] is connected to the V-Core CPU's external interrupt #1. If the input transitions from low to high, external interrupt #1 is generated (in edge-sensitive mode (TCON::IT1=1). This feature can be used in hardware-supported single-stepping. For more information, see "Debugging Features," page 118.

4.14 Dual-Data Pointers

The V-Core CPU employs dual-data pointers (SFRs) to accelerate data memory block moves. The standard 8051 data pointer SFR (DPTR) is a 16-bit value used to address external data RAM or peripherals. The V-Core CPU maintains the standard data pointer as SFR::DPTR0. It is not necessary to modify existing code to use DPTR0.

The V-Core CPU adds a second data pointer (SFR::DPTR1). The SEL bit in the DPTR Select register, DPS::SEL, selects the active pointer. When DPS::SEL is 0, instructions that use the DPTR are directed to use DPL0 and DPH0. When DPS::SEL is 1, instructions that use the DPTR are directed to use DPL1 and DPH1.

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the DPS::SEL bit. The fastest way to do this is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address; as a result, it is not necessary for the application code to save source and destination addresses when doing a block move. It is possible to use the INC instruction without side effects because the remaining bits of the DPS SFR are unused. Using dual-data pointers provides significantly increased efficiency when moving large blocks of data.

4.15 Mailbox

Synchronizing tasks between an optional external CPU attached to the device's serial interface and the V-Core CPU can be a problematic job without hardware support. The mailbox provides functionality to assist in overcoming these problems. It consists of three 32-bit chip registers that are accessible from both the V-Core CPU and an external CPU.

The CHIP::SYSTEM::ICPU_MBOX_VAL is a read-only register that returns the current value of the mailbox. Its value is changed using the event registers SYSTEM::ICPU_MBOX_SET and SYSTEM::ICPU_MBOX_CLR. All bits that are set in the value written to ICPU_MBOX_SET are also set in the ICPU_MBOX_VAL. Bits that have a 0 written to ICPU_MBOX_SET do not affect the bits in ICPU_MBOX_VAL. The same is true for the ICPU_MBOX_CLR register: All bits set in the value written to ICPU_MBOX_CLR register clear the corresponding bits in the ICPU_MBOX_VAL register. Bits that have a 0 written to ICPU_MBOX_CLR do not affect the corresponding bits of ICPU_MBOX_VAL.

To use the mailbox, it is recommended to divide the 32 bits into two or more segments, where a segment is logically assigned to each of the CPUs. One CPU sets bits in one segment, which is conveyed to the other CPU, which, in turn, clears the bits in the segment when the event is handled. This tells the first CPU that the event is handled and vice versa.

Numbers can also be transferred through the mailbox by first writing the integer as is to the ICPU_MBOX_SET register, then negating the integer bit-wise. and finally writing this new value to the ICPU_MBOX_CLR register.

Another chip-register, CHIP::SYSTEM::HWSEM, works as a semaphore, which enables performing mutual exclusions in software tasks. To obtain the semaphore, read the register and monitor the returned value. If the register returns a 1, the reader is now the owner of the semaphore. If it is 0, the semaphore is already taken by another task. To release the semaphore, write a 1 to the register.

4.16 Debugging Features

It is often convenient to have some means of debugging the code running within the V-Core CPU. This section describes a solution that uses a combination of software and hardware for debugging the code within the V-Core CPU.

4.16.1 Single-Stepping

The interrupt structure of the V-Core CPU allows for single-stepping programs. When exiting an interrupt service routine (ISR) with a RETI instruction, the V-Core CPU always executes at least one instruction of the task program. Therefore, after an ISR is entered, it cannot be re-entered until at least one program instruction is executed. To perform single-step execution, program the GPIO interrupt (external interrupt #1) to be level-sensitive and write an ISR for this interrupt that terminates as follows:

```
wait1:  JB  TCON.3, wait1 ; Wait for inactive level (high) on
                          ; external interrupt #1.
                          ; This corresponds to ICPU_GPIO[0]=0.
wait2:  JNB TCON.3, wait2 ; Wait for active level (low) on
                          ;external interrupt #1.
                          ; This corresponds to ICPU_GPIO[0]=1.
        IRET              ; Return from interrupt.
```

To enter the ISR, the ICPU_GPIO[0] pin (must be configured as input) must be set high. The ISR then performs whatever task it needs to (toggles LEDs or the like to indicate to the user that the ISR is entered) and finishes the ISR by first waiting for 0 and then for 1 on the GPIO input. As soon as the IRET instruction and one more instruction are executed, the ISR is re-entered, effectively causing just one user-instruction to be executed.

If the ICPU_GPIO[0] pin is connected to a glitch-free switch or button, the user can single-step through the program using this switch.

4.16.2 External Access to On-Chip RAMs

The single-stepping procedure outlined in the previous section can be combined with an external CPU reading the contents of the on-chip RAMs in each step. The external CPU, which is attached to the SparX-G5e serial interface, can gain complete control over both the eight kilobytes of on-chip RAM and the scratchpad RAM through the two chip-registers: SYSTEM::ICPU_ADDR and SYSTEM::ICPU_DATA.

Continuing the example from the previous section about single-stepping, an external CPU may now take over the on-chip RAMs, while the ISR is waiting for the ICPU_GPIO[0] to become active again by performing the following steps:

1. Stop the V-Core CPU clock by writing 0 to CHIP::SYSTEM::ICPU_CTRL::CLK_EN.
2. Enable external access to the on-chip RAMs by writing 1 to CHIP::SYSTEM::ICPU_CTRL::EXT_ACC_EN.

The effect of the previous steps is that the on-chip CPU is temporarily halted and the external CPU has both read and write access to both on-chip RAMs.

To read the data from the eight kilobytes of the on-chip RAM, write the start-address (0-based) to SYSTEM::ICPU_ADDR::ADDR while keeping the SYSTEM::ICPU_ADDR::SP_SELECT cleared.

Then read the contents from the RAM by successively reading the SYSTEM::ICPU_DATA register. Each read returns 1 byte of data from the RAM and automatically increments the address register by 1. The 256 bytes of on-chip scratchpad RAM can be read by setting the SYSTEM::ICPU_ADDR::SP_SELECT bit to 1 while specifying the start-address.

Loading new data into the RAMs is done in much the same way as reading data from the RAMs. However, instead of reading the SYSTEM::ICPU_DATA register, the software must write to this register 1 byte at a time. As with reads, writing to the RAM also causes the address to automatically increment by 1.

When the external CPU has completed reading or writing to the on-chip RAMs, it allows the V-Core CPU to continue operation by performing the two writes to ICPU_CTRL mentioned previously, but this time it is done in reverse order: writing 0 to EXT_ACC_EN and writing 1 to CLK_EN.

The possibility of having external access to the on-chip RAM can also be used in the configuration where both ICPU_PI_En and ICPU_SI_Boot_En are strapped low. In this setup, the V-Core CPU is disabled by default after a chip reset. However, an external CPU may use the SYSTEM::ICPU_ADDR and SYSTEM::ICPU_DATA registers to load a program into the on-chip RAM and then write to the SYSTEM::ICPU_CTRL register to release the V-Core CPU from reset. However, if the V-Core CPU resets itself in this mode, it will require external assistance to get out of reset again.

5 Feature Descriptions

The purpose of this section is to describe enabling and configuring SparX-G5e for various common applications.

5.1 Spanning Tree Protocol

This section describes how the various Spanning Tree Protocol states—disabled, blocking, listening, learning, forwarding—are supported in SparX-G5e. According to the IEEE Std 802.1D standard, the Spanning Tree Protocol states have the properties listed in the following table.

Table 31. Spanning Tree Protocol Port State Properties

State	BPDU reception	BPDU generation	Frame forwarding	SMAC learning
Disabled	No	No	No	No
Blocking	Yes	No	No	No
Listening	Yes	Yes	No	No
Learning	Yes	Yes	No	Yes
Forwarding	Yes	Yes	Yes	Yes

These states can all be configured in SparX-G5e through the CAPENAB, CAPCTRL, SRCMASKS, and LERNMASK registers.

The following table lists how the portId for a port is configured to the different states. In addition, CAPCTRL::BPDU_Q can be used to configure in which CPU queue the BPDUs are placed.

Table 32. Spanning Tree Protocol Port State Configuration of SparX-G5e for Port portId

State	CAPENAB::BPDU[1]	SRCMASKS, mask portId	LERNMASK, bit portId
Disabled	1	0	0
Blocking	1	0	0
Listening	1	0	0
Learning	1	0	1
Forwarding	1	1 except for bit portId	1

1. The CPU must filter BPDUs when the ingress port is disabled.

5.1.1 Multiple Spanning Tree Protocol

SparX-G5e supports the Multiple Spanning Tree Protocol except when a port is in the learning state for a Spanning Tree instance. The switch is not learning on that port for the given Spanning Tree instance. However, this has limited impact because when the port is taken to the forwarding state, learning is done at wire-speed and, as a result, the SMAC learn delay is less important. Multiple Spanning Trees are supported for all VLANs.

To enable the various port states, the switch must be VLAN-aware. All VLAN masks written to the VLAN table must have the VLANACCESS::VLAN_SRC_CHK bit set. In addition, the switch must have the ADVLEARN::VLAN_CHK bit set, and a port must be configured as described for the forwarding state in Table 31, page 121. Port states per VLAN are then solely configured through the VLAN masks.

The following table lists the special settings that enable the different port states in Table 31 per VLAN.

Table 33. Multiple Spanning Tree Protocol Port State Configuration of SparX-G5e

State per VLAN	Action
Disabled	Port removed from VLAN mask for the particular VLAN
Blocking	Port removed from VLAN mask for the particular VLAN
Listening	Port removed from VLAN mask for the particular VLAN
Learning	Port removed from VLAN mask for the particular VLAN
Forwarding	Port added to VLAN mask for the particular VLAN

For all Spanning Tree instances, BPDUs are forwarded to the CPU independently of the port states. It is therefore up to the CPU to filter unnecessary BPDUs.

5.2 VLAN and Provider Bridge Applications

This section discusses configuring and operating the chip as both a VLAN-aware switch and a Q-in-Q enabled provider bridge.

5.2.1 Standard VLAN Operation

In a VLAN-aware switch, each port is a member of one or more virtual LANs. Each incoming frame must be assigned a VLAN membership and forwarded according to the assigned VID. The following information draws on the definitions and principles of operations in IEEE Std 802.1Q. Note that the switch supports more features than mentioned in the following section, which only describes the basic requirements for a VLAN-aware switch.

The switch is enabled for VLANs per port where the following parameters must be set:

- MAC_CFG::VLAN_AWR=1, MAC_CFG::VLAN_DBLAWR=0.
- CAT_VLAN_MISC::VLAN_TCI_IGNORE_ENA=0, CAT_VLAN_MISC::VLAN_KEEP_TAG_ENA=0.

Each port has an Acceptable Frame Type parameter, which is set to Admit Only VLAN-tagged frames or Admit All Frames:

- Admit Only VLAN-tagged frames: CAT_DROP::DROP_UNTAGGED_ENA=1, CAT_DROP::DROP_TAGGED=0.
- Admit All Frames: CAT_DROP::DROP_UNTAGGED_ENA=0, CAT_DROP::DROP_TAGGED=0.

Frames that are not discarded are then subject to the VLAN classification. Untagged and priority-tagged frames are classified to a port VLAN identifier (PVID). The PVID is per-port configured in CAT_PORT_VLAN::VLAN_VID. Tagged frames are classified to the VID given in the frame's tag.

Each port has an ingress filter parameter that, when set, discards frames that are classified to a VLAN, which is not member of the set of VLANs where the port is a member. Ingress filtering is enabled per port in register VLANMASK. To ensure that ingress filtered frames are not learned, ADVLEARN::VLAN_CHK must be set.

Forwarding in the switch is always based on the VID and the destination MAC address in combination. By default, all ports are members of all VLANs. This can be changed in VLANACCESS and VLANTIDX where port masks per VLAN are set up.

SparX-G5e can be configured for either shared VLAN learning or independent VLAN learning (default). Shared VLAN learning, where multiple VLANs map to the same filtering database, is enabled through filter identifiers (FIDs). This means that learning is unique for a (MAC, FID) set and that a learned MAC address can be seen for all VIDs that map to the FID. Shared VLAN learning is enabled in AGENCTRL::FID_MASK. The 12-bit FID mask sets which bits in the VID that are indifferent to the learning. For example, if the least significant two bits are set in the FID mask, the VID set (0xXY0, 0xXY1, 0xXY2, 0xXY3) is sharing learning, where X and Y are any hexadecimal digits.

Each egress port can configure an untagged set that defines the VIDs for which frames are transmitted untagged. For all other VIDs, frame are transmitted tagged. These are the available configurations:

- The untagged set is empty: TXUPDCFG::INSERT_TAG=1, TXUPDCFG::TX_UNTAGGED_VID_ENA=0.
- The untagged set consists of all VIDs: TXUPDCFG::INSERT_TAG=0.
- The untagged set consists of one VID <VID>: TXUPDCFG::INSERT_TAG=1, TXUPDCFG::TX_UNTAGGED_VID_ENA=1, TXUPDCFG::TX_UNTAGGED_VID=<VID>.

GARP VLAN registration protocol (GVRP) is used to propagate VLAN configurations between bridges. On a GVRP-enabled switch, all GVRP frames must be redirected to the CPU for further processing. The GVRP frames use a reserved GARP MAC address (01-80-C2-00-00-21) and can be redirected to the CPU by setting bit 1 in the analyzer in CAPENAB::GARP.

5.2.2 Provider Bridges and Q-in-Q Operation

SparX-G5e has support for some of the Provider Bridge features currently being standardized in IEEE Std 802.1ad ("Provider Bridges"). The features related to Provider Bridge that are available in SparX-G5e are:

- Support for multiple tag headers (EtherType 0x8100 recognized as the tag header EtherType).
- Enabling or disabling learning per VLAN.

The following section discusses briefly how to configure these different features in the switch.

5.2.2.1 Multiple Tag Headers

SparX-G5e supports multiple VLAN tags and can therefore be used in MAN applications as a provider bridge, aggregating traffic from numerous independent customer LANs into the MAN space. One of the purposes of the provider bridge is to recognize and use VLAN tags so that VLANs in the MAN space can be used independently from the customer's VLANs. This is accomplished by adding a VLAN tag with a MAN-related VID for frames entering the MAN. When leaving the MAN, the tag is stripped and the original VLAN tag with the customer-related VID is again available. This provides a tunneling mechanism to connect remote VLANs through a common MAN space without interfering with the VLAN tags. All tags must use EtherType 0x8100.

The relevant configuration fields are shown in the following table.

Table 34. Relevant Configuration Fields for Multiple Tag Headers

Register Field	Description
MAC_CFG::VLAN_AWR	Allow tagged frames to be MAXLEN::MAX_LENGTH + 4 bytes long.
MAC_CFG::VLAN_DBLAWR	Allow double tagged frames to be MAXLEN::MAX_LENGTH + 8 bytes long.
CAT_VLAN_MISC::VLAN_TCI_IGNORE_ENA	Ignore any tag header in received frame during VLAN classification.
CAT_VLAN_MISC::VLAN_KEEP_TAG_ENA	Do not remove tag header from frame. Frames being tagged on an egress port then have effectively two tag headers.
CAT_PORT_VLAN	Tag header for port-based VLAN
TXUPDCFG::INSERT_TAG	Insert tag specified in the internal frame header.

The following is an example of setting up SparX-G5e as a MAN access switch with the following requirements:

- Customer ports are aggregated into a network port for tunneling through the MAN to access remote VLANs.
- Local switching between different customers' ports must be eliminated.
- Frames must be label switched from network port to correct customer port without need for MAC address learning.

The above is typically accomplished by letting each customer port have a unique PVID, which is used in the outer VLAN tag. In the MAN, the VID can then directly map the customer port from which the frame is received or to which the frame is going.

A customer port is basically VLAN unaware and VLAN classifies to a port-based VLAN. In the egress direction of the customer port, frames are transmitted untagged, which facilitates stripping the outer tag. The port must allow frames with a maximum size of 1522 bytes.

An example of the configuration of a customer port is shown in the following table.

Table 35. Customer Port Sample Configuration

Register Field and Value	Description
MAC_CFG::VLAN_AWR=1 MAC_CFG::VLAN_DBLAWR=0	Length check.
CAT_VLAN_MISC::VLAN_TCI_IGNORE_ENA=1	Do not use tag header in VLAN classification.
CAT_VLAN_MISC::VLAN_KEEP_TAG_ENA=1	Leave any tag header in frame.
CAT_PORT_VLAN::VLAN_VID=<Customer VID> CAT_PORT_VLAN::VLAN_CFI=0	Customer VID. CFI value for VLAN tag.
TXUPDCFG::INSERT_TAG=0	Do not insert tag in outgoing frames on this port.

In the ingress direction, the network port must recognize the outer VLAN tag and forward frames based on its information. In the egress direction, the network port must be able to tag frames. The maximum length is now 1526 bytes.

An example of the configuration of the network port is shown in the following table.

Table 36. Network Port Sample Configuration

Register Field and Value	Description
MAC_CFG::VLAN_AWR=1 MAC_CFG::VLAN_DBLAWR=1	Length check.
CAT_VLAN_MISC::VLAN_TCI_IGNORE_ENA=0	Use tag header in VLAN classification.
CAT_VLAN_MISC::VLAN_KEEP_TAG_ENA=0	Remove tag header from frame. Frames leaving on a customer port only contain customer tags (if any). Frames leaving on network ports have the tag reinserted.
TXUPDCFG::INSERT_TAG=1	Insert tag in outgoing frames on this port.

5.2.2.2 Learning per VLAN

In cases where a given service VLAN only has two member ports in the switch, the learning can be disabled for the particular VLAN, thereby relying on flooding as the forwarding mechanism between the two ports. This way, the MAC storage requirements can be reduced. The relevant configuration field is shown in the following table.

Table 37. VLAN Learning Configuration Field

Register Field	Description
VLANACCESS::VLAN_LEARN_DISABLED	Disable learning for this VLAN.

5.3 Port-Based Network Access Control

The port-based network access standard IEEE Std 802.1X provides a framework to implement port authentication where only authenticated ports have access to the network. Ports are initially in an unauthorized state where normal frame forwarding for the port is disabled. The port only accepts special authentication frames. Upon authorization, the network services become enabled for the port, and normal frame forwarding is possible.

The authentication is initiated by extensible authentication protocol over LAN (EAPOL) frames, which are identified by the unique bridge group address 01-80-C2-00-00-03.

The configuration of a port with respect to authentication is as follows:

- For a VLAN-unaware switch, a port is placed in the un-authenticated state by:
  - Clearing the port in the receive mask (RECVMASK).
  - Clearing the port in all destination port masks (DSTMASKS).
  - Clearing the port in all flooding masks (MFLODMSK, UFLODMSK, IFLODMSK).
- For a VLAN-aware switch, a port is placed in the un-authenticated state per VLAN by:
  - Enabling ingress filtering on the port (VLANMASK) and disabling learning for ingress filtered frames (ADVLEARN::VLAN_CHK=1).
  - Removing the port from the VLANs where authentication is required.
- EAPOL frames are redirected to the CPU by setting CAPENAB:BPDU in the analyzer.

5.4 Link Aggregation

Link aggregation (IEEE Std 802.3ad) describes a way of aggregating multiple links together to form what appears to be a single link. The goals are to increase bandwidth and to reduce the risk of link failures.

To enable link aggregation, SparX-G5e must be configured as follows:

- Redirection of link aggregation control protocol (LACP) frames to the CPU: LACP frames use the reserved Slow Protocols Multicast address (01-80-C2-00-00-02) and are redirected to the CPU by enabling CAPENAB::BPDU in the analyzer.
- Frame distribution to preserve frame ordering within a conversation: CAT_OTHER_CFG configures which IP and TCP/UDP fields to include, and AGGRCTRL configures the overall method for frame distribution. For more information about the choices for frame distribution over aggregated links, see “Link Aggregation Code,” page 71 and “Aggregation Processing,” page 80.
- Setting up link aggregation groups: There are 16 aggregation masks available in AGGRMSKS. For more information about the required steps, see “Aggregation Processing,” page 80.

Note If port mirroring is enabled and mirrors frames to a port in an aggregation group, all mirrored frames go to the mirror port without reflecting the other ports in the aggregation group.

5.5 IGMP Snooping

The Internet Group Management Protocol (IGMP) lets host and routers share information about multicast group memberships. IGMP snooping is a switch feature that monitors the exchange of IGMP messages and copies them to the CPU for further processing. The overall purpose of IGMP-snooping is to limit the forwarding of multicast frames to only ports that are a member of the multicast group.

IGMP snooping is enabled in the analyzer in CAPENAB::IGMP. Note that only IPv4 IGMP frames are recognized.

6 Registers

6.1 Command Interfaces

Through the iCPU or an external CPU attached to the SI or PI interface, it is possible to configure, monitor, and collect statistics from all parts of SparX-G5e. The set of the SparX-G5e device registers and functionality is independent of the chosen interface. In addition, the V-Core CPU, if enabled, has access to a different set of registers known as Special Function Registers (SFRs).

The PI interface and V-Core CPU are mutually exclusive. The strapping of the ICPU_PI_En pin determines which interface is enabled. For more information, see Table 26, page 96.

6.2 Device Register Space

SparX-G5e consists of several functional blocks. Some of these blocks (the port and the MII Management System) are further divided into subblocks. All subblocks within a given block are clones with equal sets of registers.

Within each subblock, an 8-bit address space exists where each address accesses 32-bits of register data.

The blocks are identified with block IDs as listed in the following table.

Table 38. Blocks

Block ID	Subblocks	Slow	Functional Block	Short Name
1	Subblock 0-4, 6	Yes	Ports	PORT
2	0	Yes	Analyzer	ANALYZER
3	0-1	Yes	MII Management	MIIM
3	2	Yes	Memory Initialization	MEMINIT
4	0-3, 4, 6, 7	No	CPU Capture Buffer	CAPTURE
5	0	Yes	Frame Arbiter	ARBITER
7	0	No	System Registers	SYSTEM

The Slow column is used only when the PI interface is enabled and refers to a property of the block that is explained in “Reading Slow Registers,” page 136.

For the ports, the subblock number is the port number (0-4, 6). The subblock number also applies to the CPU capture buffer, but not as a selector between submodules, rather as an extension to the 8-bit address space. For more information, see “Frame Capturing,” page 85.

For information about the entire set of registers, see “Overview of Registers,” page 142.

6.3 SFR Register Space

In addition to the device register space, the V-Core CPU has access to its Special Function Registers register space. The following table shows the SFRs implemented in the V-Core CPU. Registers and fields marked with an asterisk (*) are not part of a standard 8051 implementation and are detailed in subsequent sections. For a description of the remaining registers and fields, see a standard 8051 datasheet.

Table 39. SFR Register Overview

Register	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
GPIO_IN*	GPIO Input	0x80	0	0	0	0	0	0	GI1	GI0	0x00
SP	Stack Ptr	0x81									0x07
DPL0	Data Ptr 0 Lo	0x82									0x00
DPH0	Data Ptr 0 Hi	0x83									0x00
DPL1*	Data Ptr 1 Lo	0x84									0x00
DPH1*	Data Ptr 1 Hi	0x85									0x00
DPS*	Data Ptr Slct	0x86	0	0	0	0	0	0	0	SEL	0x00
PCON	Power Ctrl	0x87	SMOD0	0	1	1	GF1	GF0	STOP	IDLE	0x30
TCON	Timer 0 and 1 Ctrl	0x88	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0x00
TMOD	Timer Mode	0x89	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0x00
TL0	Timer Lo 0	0x8A									0x00
TL1	Timer Lo 1	0x8B									0x00
TH0	Timer Hi 0	0x8C									0x00
TH1	Timer Hi 1	0x8D									0x00
CKCON*	Clock Ctrl	0x8E	0	0	T2M	T1M	T0M	MD2	MD1	MD0	0x01
SPC_FNC*	Special Func	0x8F	0	0	0	0	0	0	0	WRS	0x00
GPIO_OUT*	GPIO Output	0x90	0	0	0	0	0	0	GO1	GO0	0x00
SCON	Serial Ctrl	0x98	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	0x00
SBUF	Serial Data Buf	0x99									0x00
GPIO_OE*	GPIO Outp Enbl	0xA0	0	0	0	0	0	0	GOE1	GOE0	0x00
GPIO_STAT*	GPIO Status	0xA1	0	0	0	0	0	0	GS1	GS0	0x00
WDDA*	Watchdog Data	0xA2									0xEF
WDCON*	Watchdog Ctrl	0xA3	0	0	0	0	0	0	0	WDEN	0x00
IE	Interrupt Enable	0xA8	EA	0	ET2*	ES	ET1	EX1	ET0	EX0	0x00
FPIE*	Frame Present Interrupt Enable	0xA9	0	0	0	0	0	0	Q1	Q0	0x00
FPSTAT*	Frame Present Status	0xAA	0	0	0	0	0	0	Q1	Q0	0x00
PG*	Page Register	0xB0	IFP3	IFP2	IFP1	IFP0	OP3	OP2	OP1	OP0	0x00
IP	Interrupt Priority	0xB8	1	0	PT2*	PS	PT1	PX1	PT0	PX0	0x80

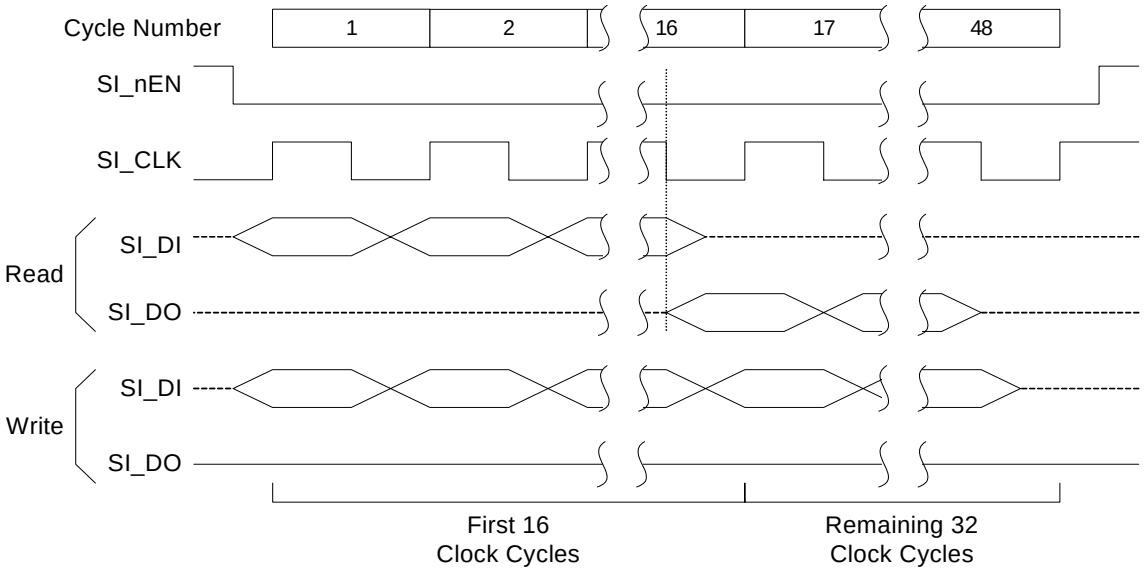
Table 39. SFR Register Overview *(continued)*

Register	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
T2CON*	Timer 2 Ctrl	0xC8	TF2	0	RCLK	TCLK	0	TR2	0	0	0x00
RCAP2L*	Timer 2 Capt Lo	0xCA									0x00
RCAP2H*	Timer 2 Capt Hi	0xCB									0x00
TL2*	Timer Lo 2	0xCC									0x00
TH2*	Timer Hi 2	0xCD									0x00
PSW	Prog Stat Word	0xD0	CY	AC	F0	RS1	RS0	OV	F1*	P	0x00
ACC	Accumulator	0xE0									0x00
B	B register	0xF0									0x00
SPC_FNC2	Special Func 2	0xF1	0	0	0	0	0	0	0	ENA	0x00
RA_DONE*	Reg Acc Done	0xF8	0	0	0	0	0	0	0	DONE	0x00
RA_BLK*	Reg Acc Block	0xF9	BL2	BL1	BL0	0	SBL3	SBL2	SBL1	SBL0	0x00
RA_AD_RD*	Reg Acc Rd Addr	0xFA									0x00
RA_AD_WR*	Reg Acc Wr Addr	0xFB									0x00
RA_DA0*	Reg Acc Data 0	0xFC									0x00
RA_DA1*	Reg Acc Data 1	0xFD									0x00
RA_DA2*	Reg Acc Data 2	0xFE									0x00
RA_DA3*	Reg Acc Data 3	0xFF									0x00
* These registers and fields are not part of a standard 8051 implementation and are detailed in subsequent sections.											

6.4 Serial Interface

The serial interface (SI) is a simple interface that operates as described in the Serial Peripheral Interface (SPI) specification by Motorola (not to be confused with SPI-4.2, which is a high-speed interface), running in mode CPHA = 0 and CPOL = 0. It consists of four signal lines: an input clock (SI_Clk), an enable signal (SI_nEn), and a data signal in each direction (SI_DI and SI_DO).

Figure 26. SI Communication



An external clock running at a speed between 0 MHz and 25 MHz clocks the interface. SI_nEn low starts an operation consisting of 48 clock cycles: 8 for command/block/subblock, 8 for address, and 32 for data. In case of a read operation, SI_DO is driven; otherwise, it is kept tri-stated.

Table 40. Block Address Structure Format

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Block ID			Write	Subblock Number			
1	Address							
2	Data							
3	Data							
4	Data							
5	Data							

6.4.1 SI Clock Select

The internal timing of SparX-G5e means that the SI user must ensure at least a 200-ns delay from when the last bit of a read address is transmitted to when SI_Clk goes low again. This can be done in three ways:

- Let the SI clock run at about 2.5 MHz or below (see Figure 27 and Figure 28).
- Let the SI clock pause (at HIGH) after the last address is clocked out (see Figure 29).
- Ask SparX-G5e to insert idle byte periods before the read data (see Figure 30).

Figure 27. SI Read Operation Sequence (Low Clock)

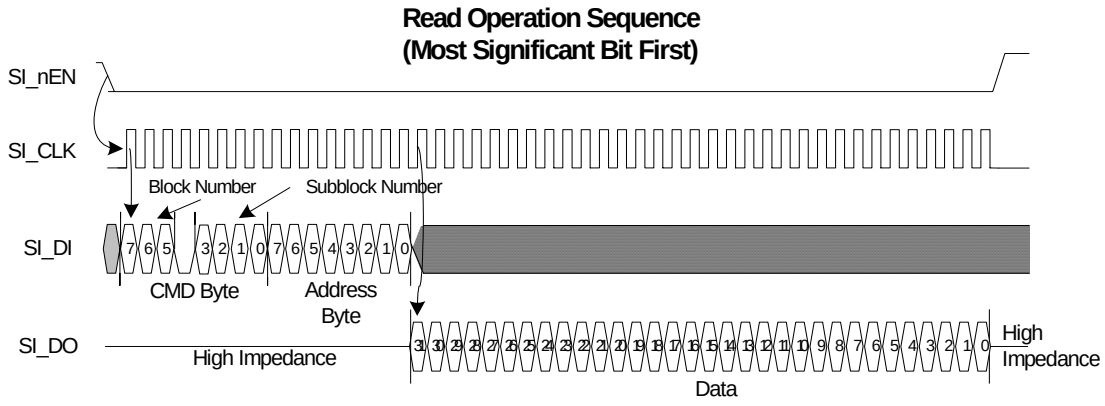


Figure 28. SI Write Operation Sequence (Low Clock)

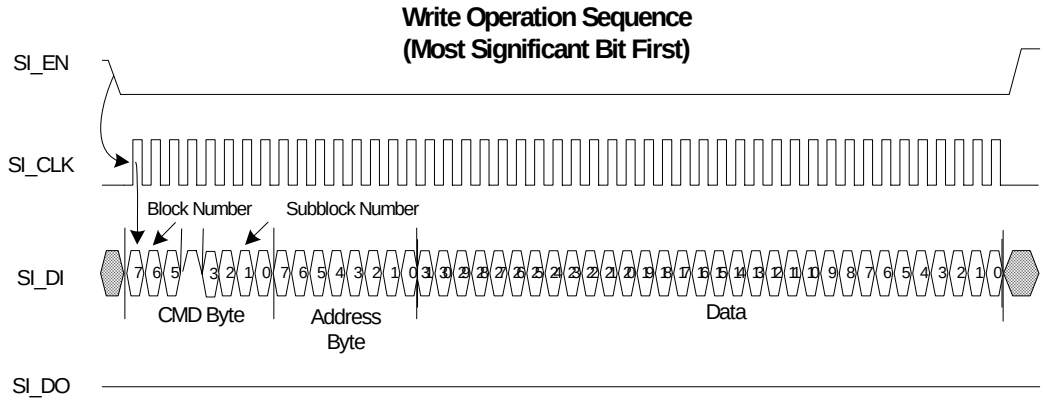


Figure 29. SI Read Operation with Clock Pause

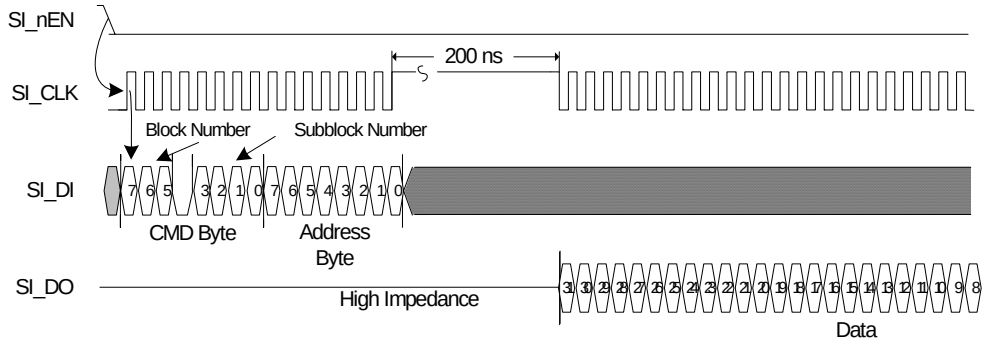
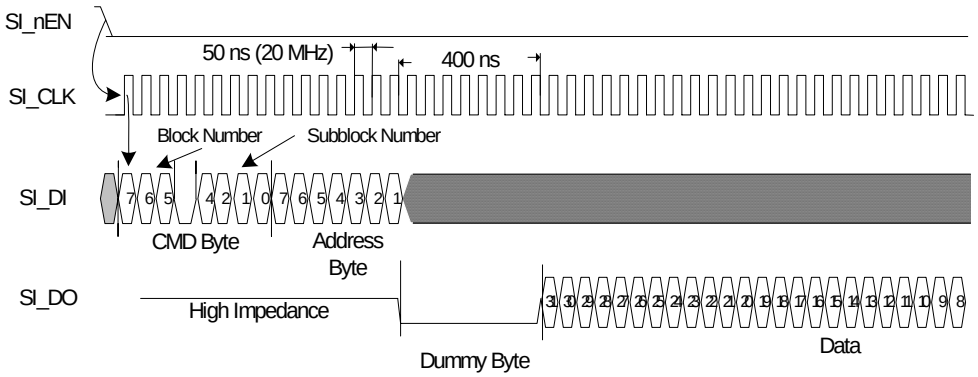


Figure 30. SI Read Operation with Dummy Byte



As an example of the third option, assume the SI clock is running at 20 MHz, which gives a clock cycle of 50 ns. To ensure a 200-ns delay before data is read out, SparX-G5e must add padding bytes (PB) so that (8 × PB + 0.5) × ClkCycle ≥ 200 ns. Therefore, to run a 20-MHz SI, one byte of extra dummy data must be inserted in the read protocol sequence between command/address and data. The following table lists the clock limits for each configuration of dummy bytes.

Table 41. Number of Dummy Bytes Versus Clock

Maximum SI Clock	Number of Dummy Bytes
2.5 MHz	0
25 MHz	1

Write operations do not contain any padding bytes no matter what padding configuration is chosen. Therefore, no special care need be taken during the initial set-up of SparX-G5e for pad insertion; this can be done at full speed.

6.4.2 SI Configuration

Using certain system registers, the SI protocol sequence can be configured to do one of the following:

- To select the byte order for the interface when sending 32-bit data words (endian selection).
- To select whether to transfer the most or the least significant bit first within each byte.
- To select the insertion of idle bytes before read data is transmitted.

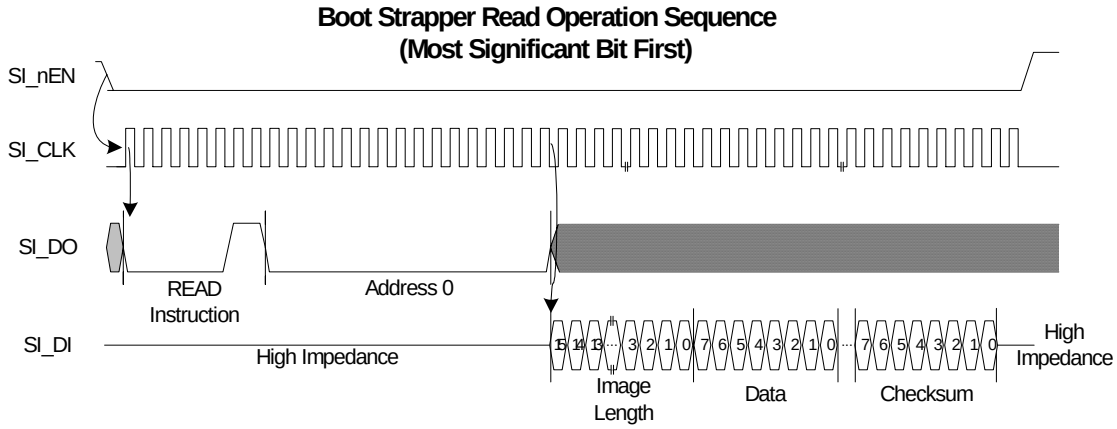
Table 42. SI Configuration Register

System Register	Description
CPUMODE	Selects endian mode and bit transfer order
SIPAD	Selects number of padding bytes

6.4.3 SI EEPROM Booting

The following figure shows the SI read operation sequence when booting from an EEPROM.

Figure 31. SI Boot Strapper Read Operation



For more information about SI EEPROM booting, see "SI EEPROM Booting," page 105.

6.5 Parallel Interface

After it is enabled, the parallel interface's access to the registers is superior in terms of speed compared to the serial interface. The interface is eight bits wide and covers an address space of 2^{15} 32-bit words.

The interface consists of 8 data pins, 17 address pins, 3 control pins, and 1 handshake or acknowledge pin. In addition, there are two interrupt pins, whose purpose is to notify the external CPU about specific events, but they are not directly part of the interface protocol. The interface supports automatic byte addressing, where only the word selecting address lines are connected to the switch. The various pins are described in the following table.

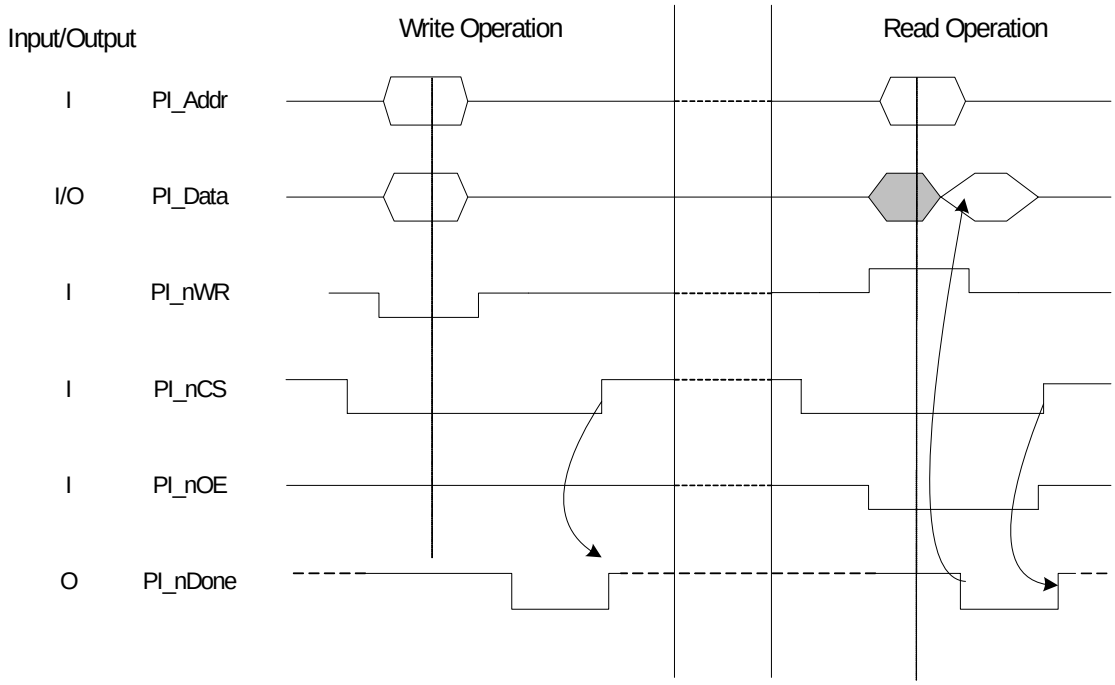
Table 43. Parallel Interface Signals

PI Signal	Direction	Width	Description
PI_Addr	I	17	Selects the block, subblock, and address as well as the part of a 32-bit register accessed.
PI_Data	I/O	8	Driven by CPU at write and by SparX-G5e at read.
PI_nWR	I	1	Selects read (1) or write (0).
PI_nOE	I	1	Enables drive of the data bus from SparX-G5e.
PI_nCS	I	1	Starts a CPU operation.
PI_nDone	OZ	1	Acknowledges an operation.
PI_IRQ	O	2	Indicates two configurable interrupt signals for various events.

The operations of the interface are shown in the following figure. To use the interface, do the following:

1. Lower the nCS signal.
2. Within 20 ns, set up address, R/W select and data in case of write operation.
3. Wait until at least 50 ns from when nCS was lowered or wait for nDone to fall.
4. Store data from the data bus in case of read operation.
5. Raise the nCS signal.

Figure 32. PI Communication



All inputs are latched a configurable amount of time after nCS falling. The delay is set in the CPUCTRL register and is configurable from 10 ns to 200 ns with 200 ns as the default. nDone acknowledges the operation approximately 10 ns later. For more information about precise timing, see the AC Specifications for the "AC Specifications for PI (Parallel CPU Interface)," page 235.

The nOE signal along with the nCS signal directly control the output driver of the data bus.

6.5.1 Reading Slow Registers

Most of the registers in SparX-G5e have a larger access time than might be acceptable for a CPU bus cycle. The access time can be up to 200 ns, and therefore special action must be taken to read the registers as shown in the following sections.

6.5.1.1 Using the SLOWDATA Postponed Result

One method of coping with the slow read result is to make a dummy read from the target register without using the result, use the read delay time for something else by the software, and read the SLOWDATA register after the read delay is passed.

This method is shown in the following example.

1. Read the register (only the first-byte access).
2. Poll the SlowDone bit of CPUCTRL, wait for SlowDone interrupt, or ensure a delay of at least 200 ns.
3. Read the SLOWDATA register.

Use the CPUCTRL::EXT_USE_SLOW field to enable this feature.

6.5.1.2 Extended Bus Cycle

It is also possible to extend the bus cycle, thereby postponing the nDone handshake until slow data is available. In this mode, all registers are read like fast registers, but the nDone signal is not activated until up to 200 ns after the falling nCS signal. The extended bus cycle is default behavior and can be disabled through the CPUCTRL register. Only the first byte access to a slow register has a long access time.

6.5.2 Interrupt Control

The PI_IRQ pins of SparX-G5e can be used to signal when a CPU should take action on two different events: when the SLOWDATA register is filled or when a frame is ready in the CPU frame receive buffer. The interrupt signal is of level type and is cleared when the source condition inside SparX-G5e is removed by reading the SLOWDATA register or by acknowledging a CPU frame.

6.5.3 Register Addressing

The SparX-G5e registers are mapped into the 17-bit address space of the PI, as shown in the following table.

Table 44. Register Mapping in PI Address Space

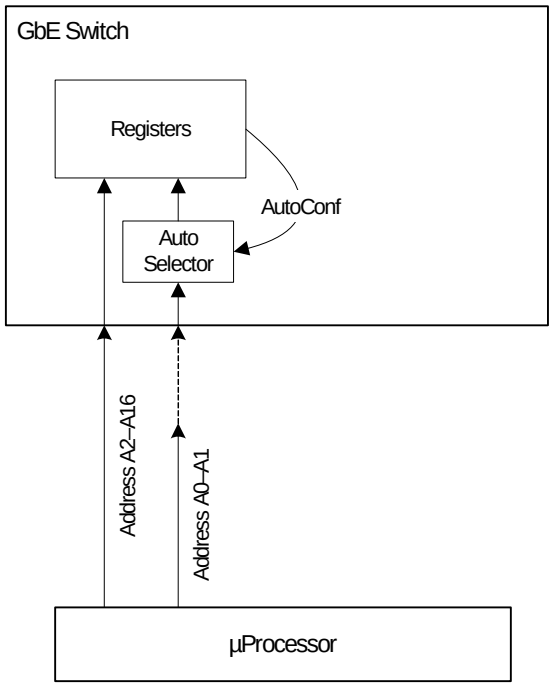
A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Block ID			Subblock Number				Register address								WS	BS

The BS/WS pins select the part of the 32-bit word to access. When the interface is running in big-endian mode (default), the BS/WS pins select the least significant part of the word, and in little endian mode, it selects the most significant part.

6.5.4 Auto Word and Byte Selection

The two word and byte selection pins can be set in auto mode. In this mode, it is then not necessary to connect them to the CPU. In auto mode, the interface logic assumes accesses from lower to higher addresses.

Figure 33. Auto Address Bus



As an example, system register 0 is read (big-endian mode), as shown in the following table. The address of this register is found through the mapping seen in the PI mapping table. The System block has blockId 7 and subblock number 0. As a result, the 17-bit address to this register is 0x1C000, and the following table shows the four accesses with an 8-bit bus.

Table 45. PI Bus 8-Bit Data Width Example

Access Number	CPU Bus Address / Non-Auto Mode	CPU Bus Address / Auto Mode	Data
0	0x1C000	0x1C000	Most significant byte
1	0x1C001	0x1C000	Second most significant byte
2	0x1C002	0x1C000	Second least significant byte
3	0x1C003	0x1C000	Least significant byte

6.5.5 PI Mode Setup

A special register exists inside the PI controller, which sets up width and auto properties. The register PICONF is the only 8-bit register in the device and is accessed in a single cycle. The register is write only (W/O) and is used for selecting auto mode for the A0 and A1 pins.

6.6 Minimum Software Requirements

The SparX-G5e device is almost fully working with its default configuration. The minimum set of registers to set up for basic operation is listed in the following table. For more information about using statistics, aggregation, VLAN, flow control, MAC aging, and so forth, see "Overview of Registers," page 142.

Table 46. Minimum Register Set to Use

Register Name	Use for
MEMINIT	Initializing memories
MACACCESS	Formatting MAC table
VLANACCESS	Formatting VLAN table
MAC_CFG	Setting the port mode according to PHY status
RECVMASK	Enabling frame forwarding from ports
MIIMCMD	Performing a MII management operation
MIIMDATA	Reading PHY read results from MII management operation
GLORESET	Releasing reset of PHYs

The mandatory operation for the software is split into an initialization sequence and a PHY polling operation. If the PHYs are running with fixed speed and duplex mode, the poll operation can be ignored, and the SparX-G5e ports can be set to the desired mode as a part of the initialization sequence.

The following simple routines are only for showing the minimum requirements and cannot be used as the basis for a final software system. They are added here to introduce using the chip registers.

Note The register accesses use the format: block.subblock.address.

6.6.1 Initialization Sequence

The following initialization sequence is *required* to ensure proper operation of the switch. The V-Core CPU may use both the scratchpad RAM and eight-kilobytes on-chip RAM while the following code sample is executed.

Initialization Sequence

```
/* Initialize memories */
for (memId=0; memId<=15; memId++){
  if (memId!=6 && memId!=7) {
    Write(MEMINIT.2.MEMINIT, 0x1010400 + memId);
    Sleep 1 ms;
  }
}
Sleep 30 ms;

/* Format memories */
Write(ANALYZER.0.MACACCESS, 5); /* CLEAR MAC TABLE command */
Write(ANALYZER.0.VLANACCESS, 3); /* CLEAR VLAN TABLE command */
Sleep 40 ms;

/* Use 20-kilobyte buffers on all ports */
Write(PORT.31.Q_MISC_CONF, 0x80000000);

/* Release reset of PHY's */
Write(SYSTEM.0.GLORESET, 2);

Sleep 4 µs
```

A PHY initialization sequence should also be used to re-enable the PHYs after a soft or hard reset of the PHYs, or after manual power-down. For more information about the PHY initialization sequence, see the *AN0089 VSC7395 VSC7398 PHY Configuration* application note.

6.6.2 Port Mode Procedure

Execute this procedure on a regular basis for updating the port mode according to the PHY state. This example illustrates the basic requirements only but must be expanded for a real software control program. For more information about a fully detailed procedure, see the SparX-G5e software source code.

Port Mode Procedure

```
for (portId=0; portId<6; portId++) {
  /* Use MIIMCMD and MIIMDATA to retrieve current speed
     and link status from PHY attached to port <portId>
     Put the status into the <mode>
  */

  /* Map portId to macId */
  macId = PortId_to_MacId(portId);

/* Enable forwarding from a port, only if the port link is up */
  if (mode==DOWN)
    Write(ANALYZER.0.RECVMASK, Read(ANALYZER.0.RECVMASK) & ~(1<<macId));
  else
    Write(ANALYZER.0.RECVMASK, Read(ANALYZER.0.RECVMASK) | (1<<macId));

  /* Set the port MAC to the current mode */
  switch (mode) {
    case DOWN:     Write(PORT.macId.MAC_CFG, 0x20000030); break;
    case 1GFULL:   Write(PORT.macId.MAC_CFG, 0x10070184); break;
    case 100MFULL: Write(PORT.macId.MAC_CFG, 0x10050444); break;
    case 10MFULL:  Write(PORT.macId.MAC_CFG, 0x10050444); break;
    case 100MHALF: Write(PORT.macId.MAC_CFG, 0x90010444); break;
    case 10MHALF:  Write(PORT.macId.MAC_CFG, 0x90010444); break;
  }
}
```

6.7 Overview of Registers

The following section provides a list of the registers in the SparX-G5e device.

6.7.1 System Block Registers

Table 47. System Block Registers (Block 7)

Address	Register Name	Short Name	Details
0x00	CPU Transfer Mode	CPUMODE	Page 150
0x01	SI Padding	SIPAD	Page 150
0x02	PI Config	PICONF	Page 151
0x05	GMII Clock Delay	GMIIDELAY	Page 151
0x13	Semaphore Register	HWSEM	Page 151
0x14	Global Reset	GLORESET	Page 152
0x18	Chip Identification	CHIPID	Page 152
0x24	Time Compare Value	TIMECMP	Page 153
0x2C	Slow Data	SLOWDATA	Page 153
0x30	CPU Control	CPUCTRL	Page 153
0x31	Capture Control	CAPCTRL	Page 154
0x34	General-Purpose I/O	GPIO	Page 154
0x35	SI Master Interface	SIMASTER	Page 155

6.7.2 V-Core CPU Block Registers

Table 48. V-Core CPU Block Registers (Block 7)

Address	Register Name	Short Name	Details
0x10	Internal CPU Control	ICPU_CTRL	Page 156
0x11	Internal CPU On-Chip RAM Address	ICPU_ADDR	Page 157
0x12	Internal CPU On-Chip RAM Data	ICPU_DATA	Page 157
0x15	Mailbox Value	ICPU_MBOX_VAL	Page 158
0x16	Mailbox Set	ICPU_MBOX_SET	Page 158
0x17	Mailbox Clear	ICPU_MBOX_CLR	Page 158
0x19	External Data Memory Access Control Configuration	ICPU_RAM_CFG	Page 158
0x1A	External Program Memory Access Control Configuration	ICPU_ROM_CFG	Page 159
0x1B	On-Chip RAM Mapping in Data Memory Space	ICPU_RAM_MAP	Page 159
0x1C	On-Chip RAM Mapping in Code Memory Space	ICPU_ROM_MAP	Page 160

6.7.3 PORTREG Block Registers

Table 49. PORTREG Block Registers (Block 1)

Address	Register Name	Short Name	Details
0x01	Device Register Mode	REGMODE	Page 161

6.7.4 MAC Block Registers

Table 50. MAC Block Registers (Block 1)

Address	Register Name	Short Name	Details
0x00	MAC Configuration	MAC_CFG	Page 161
0x02	Half-Duplex Gaps	MACHDXGAP	Page 162
0x04	Flow Control Setup	FCCONF	Page 163
0x08	Flow Control SMAC High	FCMACHI	Page 163
0x0C	Flow Control SMAC Low	FCMACLO	Page 163
0x10	Maximum Length	MAXLEN	Page 163
0x19	Advanced Port Mode Setup	ADVPORTM	Page 164
0x28	Tx Queue Selector Configuration	TXQ_SELECT_CFG	Page 164
0x24	Transmit Modify Setup	TXUPDCFG	Page 165

6.7.5 Shared FIFO Block Registers

Table 51. Shared FIFO Block Registers (Block 1)

Address	Register Name	Short Name	Details
0xC0	CPU Transmit DATA	CPUTXDAT	Page 166
0xC4	Miscellaneous Control Register	MISCFIFO	Page 166
0xC8	Miscellaneous Status	MISCSTAT	Page 166
0xD8	Free RAM Counter	FREEPOOL	Page 166
0xDE	Flow Control Watermarks	Q_FLOWC_WM	Page 167
0xDF	Miscellaneous Pool Control	Q_MISC_CONF	Page 167
0xE0	Drop Watermarks	Q_DROP_WM	Page 167

6.7.6 Categorizer Block Registers

Table 52. Categorizer Block Registers (Block 1)

Address	Register Name	Short Name	Details
0x6E	Categorizer Frame Dropping	CAT_DROP	Page 168

Table 52. Categorizer Block Registers (Block 1) *(continued)*

Address	Register Name	Short Name	Details
0x6F	Categorizer Miscellaneous Layer-2 QoS	CAT_PR_MISC_L2	Page 168
0x75	Categorizer User Priority	CAT_PR_USR_PRIO	Page 169
0x60	Categorizer DSCP QoS	CAT_PR_DSCP_QOS	Page 169
0x61	Categorizer DSCP Values 0-3	CAT_PR_DSCP_VAL_0_3	Page 169
0x62	Categorizer DSCP Values 4-6	CAT_PR_DSCP_VAL_4_6	Page 170
0x77	Categorizer Miscellaneous Layer-3 QoS	CAT_PR_MISC_L3	Page 170
0x79	Categorizer VLAN Miscellaneous	CAT_VLAN_MISC	Page 171
0x7A	Categorizer Port VLAN	CAT_PORT_VLAN	Page 171
0x7B	Categorizer Other Configuration	CAT_OTHER_CFG	Page 171
0x7D	Categorizer Generic Priority Remap	CAT_GENERIC_PRIO_REMAP	Page 171

6.7.7 Detailed Counters Block Registers

Table 53. Detailed Counters Block Registers (Block 1)

Address	Register Name	Short Name	Details
0x50	Rx Octets	C_RXOCT	Page 172
0x51	Tx Octets	C_TXOCT	Page 172
0x52	Rx Counter 0	C_RX0	Page 172
0x53	Rx Counter 1	C_RX1	Page 172
0x54	Rx Counter 2	C_RX2	Page 172
0x55	Tx Counter 0	C_TX0	Page 173
0x56	Tx Counter 1	C_TX1	Page 173
0x57	Tx Counter 2	C_TX2	Page 173
0x58	Counter Control Configuration	CNT_CTRL_CFG	Page 173

6.7.8 MII Management Bus Block Registers

Table 54. MII Management Bus Block Registers (Block 3)

Address	Register Name	Short Name	Details
0x00	MII-M Status	MIIMSTAT	Page 175
0x01	MII-M Command	MIIMCMD	Page 175
0x02	MII-M Return Data	MIIMDATA	Page 176
0x03	MII-M Prescaler	MIIMPRES	Page 176
0x04	MII-M Scan Setup	MIIMSCAN	Page 176
0x05	MII-M Scan Results	MIIMSRES	Page 176

6.7.9 Memory Initialization Block Registers

Table 55. Memory Initialization Block Registers (Block 3)

Address	Register Name	Short Name	Details
0x00	Initialize	MEMINIT	Page 177

6.7.10 Frame Arbiter Block Registers

Table 56. Frame Arbiter Block Registers (Block 5)

Address	Register Name	Short Name	Details
0x0C	Arbiter Empty	ARBEMPTY	Page 177
0x0E	Arbiter Discard	ARBDISC	Page 177
0x12	Backward for Source	SBACKWDROP	Page 177
0x13	Backward for Destination	DBACKWDROP	Page 178
0x15	Burst Probability	ARBBURSTPROB	Page 178

6.7.11 CPU_CAPT Block Registers

Table 57. CPU_CAPT Block Registers (Block 4)

Address	Register Name	Short Name	Details
0x00	Frame Data	FRAME_DATA	Page 179

6.7.12 CPU_CAPT_CTRL Block Registers

Table 58. CPU_CAPT_CTRL Block Registers (Block 4)

Address	Register Name	Short Name	Details
0x00	Read Pointer	CAPREADP	Page 179
0x03	Write Pointer	CAPWRP	Page 179

6.7.13 CPU_CAPT_RST Block Registers

Table 59. CPU_CAPT_RST Block Registers (Block 4)

Address	Register Name	Short Name	Details
0xFF	Full Reset	CAPRST	Page 180

6.7.14 Frame Analyzer Block Registers

Table 60. Frame Analyzer Block Registers (Block 2)

Address	Register Name	Short Name	Details
0x02	Flooding Storm Control	STORMLIMIT	Page 180
0x03	Advanced Learning Setup	ADVLEARN	Page 180
0x04	IP Multicast Flood Mask	IFLODMSK	Page 181
0x05	VLAN Source Port Mask	VLANMASK	Page 181
0x06	MAC Address High	MACHDATA	Page 181
0x07	MAC Address Low	MACLDATA	Page 181
0x08	Station Move Logger	ANMOVED	Page 182
0x09	Aging Filter	ANAGEFIL	Page 182
0x0A	Event Sticky Bits	ANEVENTS	Page 182
0x0B	Event Sticky Mask	ANCNTMSK	Page 183
0x0C	Event Sticky Counter	ANCNTVAL	Page 183
0x0D	Learn Mask	LEARNMASK	Page 184
0x0E	Unicast Flood Mask	UFLODMSK	Page 184
0x0F	Multicast Flood Mask	MFLODMSK	Page 184
0x10	Receive Mask	RECVMASK	Page 184
0x20	Aggregation Mode	AGGRCTRL	Page 184
0x30	Aggregation Masks	AGGRMSKS	Page 185
0x40	Destination Port Masks	DSTMASKS	Page 185
0x80	Source Port Masks	SRCMASKS	Page 185
0xA0	Capture Enabled	CAPENAB	Page 185
0xB0	MAC Table Command	MACACCESS	Page 186
0xB1	IPMC Access	IPMCACCESS	Page 187
0xC0	MAC Table Index	MACTINDX	Page 187
0xD0	VLAN Table Command	VLANACCESS	Page 187
0xE0	VLAN Table Index	VLANTIDX	Page 188
0xF0	Analyzer Configuration Register	AGENCTRL	Page 188

6.7.15 Standard Set Block Registers (PHY)

Table 61. Standard Set Block Registers (PHY Registers)

Address	Register Name	Short Name	Details
0x00	Control	PHY_CTRL	Page 188
0x01	Status	PHY_STAT	Page 189
0x02	Identifier Number 1	PHY_IDF1	Page 190

Table 61. Standard Set Block Registers (PHY Registers) *(continued)*

Address	Register Name	Short Name	Details
0x03	Identifier Number 2	PHY_IDF2	Page 190
0x04	Auto-Negotiation Advertisement	PHY_AUTONEG_ADVERTISMENT	Page 190
0x05	Auto-Negotiation Link Partner Base Page Ability	PHY_AUTONEG_LP_ABILITY	Page 191
0x06	Auto-Negotiation Expansion	PHY_AUTONEG_EXP	Page 191
0x07	Auto-Negotiation Next Page Transmit	PHY_AUTONEG_NEXTPAGE_TX	Page 192
0x08	Auto-Negotiation LP Received Next Page	PHY_AUTONEG_NEXTPAGE_RX	Page 192
0x09	1000BASE-T Control	PHY_CTRL_1000BT	Page 193
0x0A	1000BASE-T Status	PHY_STAT_1000BT	Page 193
0x0F	Extended Status	PHY_STAT_EXT	Page 194
0x10	100BASE-TX Status	PHY_STAT_100BTX	Page 194
0x11	Extended 1000BASE-T Status	PHY_STAT_1000BT_EXT	Page 195
0x12	Bypass Control	PHY_BYPASS_CTRL	Page 195
0x16	Extended Control and Status	PHY_CTRL_STAT_EXT	Page 196
0x17	Extended Control Number 1	PHY_CTRL_EXT1	Page 198
0x18	Extended Control Number 2	PHY_CTRL_EXT2	Page 198
0x1B	LED Control	PHY_LED_CTRL	Page 200
0x1C	Auxiliary Control and Status	PHY_AUX_CTRL_STAT	Page 200
0x1D	Delay Skew Status Register	DELAY_SKEW_STAT	Page 202
0x1E	LED Behavior Control	PHY_LED_BEHAVIOR_CTRL	Page 203
0x1F	Memory Page Access	PHY_MEMORY_PAGE_ACCESS	Page 203

6.7.16 Extended Set Block Registers (PHY)

Table 62. Extended Set Block Registers (PHY Registers)

Address	Register Name	Short Name	Details
0x14	Extended Control Number 3	PHY_CTRL_EXT3	Page 204
0x17	Extended Control Number 4	PHY_CTRL_EXT4	Page 205
0x18	VeriPHY Control	PHY_VERIPHY_CTRL	Page 206
0x1D	1000BASE-T Ethernet Packet Generator Number 1	PHY_1000BT_EPG1	Page 206
0x1E	1000BASE-T Ethernet Packet Generator Number 2	PHY_1000BT_EPG2	Page 207

6.7.17 General-Purpose I/O SFR Registers

Table 63. General-Purpose I/O SFR Registers

Address	Register Name	Short Name	Details
0x80	General-Purpose I/O Input	GPIO_IN	Page 207

Table 63. General-Purpose I/O SFR Registers *(continued)*

Address	Register Name	Short Name	Details
0x90	General-Purpose I/O Output	GPIO_OUT	Page 208
0xA0	General-Purpose I/O Output Enable	GPIO_OE	Page 208
0xA1	General-Purpose I/O Status	GPIO_STAT	Page 208

6.7.18 Dual-Data Pointer SFR Registers

Table 64. Dual-Data Pointer SFR Registers

Address	Register Name	Short Name	Details
0x84	Data Pointer 1 Low	DPL1	Page 209
0x85	Data Pointer 1 High	DPH1	Page 209
0x86	Data Pointer Select	DPS	Page 209

6.7.19 Memory Access Control SFR Registers

Table 65. Memory Access Control SFR Registers

Address	Register Name	Short Name	Details
0x8F	Special Function Register	SPC_FNC	Page 209
0xB0	Paging Control	PG	Page 210
0xF1	Access Internal Flash as External RAM	SPC_FNC2	Page 210

6.7.20 Frame Present SFR Registers

Table 66. Frame Present SFR Registers

Address	Register Name	Short Name	Details
0xA9	Enable CPU Capture RAM Interrupts	FPIE	Page 210
0xAA	CPU Capture RAM Frame Present Status	FPSTAT	Page 211

6.7.21 Watchdog SFR Registers

Table 67. Watchdog SFR Registers

Address	Register Name	Short Name	Details
0xA2	Watchdog Data	WDDA	Page 211
0xA3	Watchdog Control	WDCON	Page 211

6.7.22 Additional Timer-Related SFR Registers

Table 68. Additional Timer-Related SFR Registers

Address	Register Name	Short Name	Details
0x8E	Timer Clock and External Memory Stretch Cycles Control	CKCON	Page 212
0xA8	Interrupt Enable	IE	Page 212
0xB8	Interrupt Priority	IP	Page 213
0xC8	Timer 2 Control	T2CON	Page 213
0xCA	Timer 2 Capture Low	RCAP2L	Page 214
0xCB	Timer 2 Capture High	RCAP2H	Page 214
0xCC	Timer 2 Low	TL2	Page 214
0xCD	Timer 2 High	TH2	Page 214

6.7.23 Chip Register Access SFR Registers

Table 69. Chip Register Access SFR Registers

Address	Register Name	Short Name	Details
0xF8	Register Access Done	RA_DONE	Page 215
0xF9	Register Access Block and Subblock	RA_BLK	Page 215
0xFA	Register Access Read Address	RA_AD_RD	Page 215
0xFB	Register Access Writer Address	RA_AD_WR	Page 215
0xFC	Register Access Data Byte Number 0	RA_DA0	Page 215
0xFD	Register Access Data Byte Number 1	RA_DA1	Page 216
0xFE	Register Access Data Byte Number 2	RA_DA2	Page 216
0xFF	Register Access Data Byte Number 3	RA_DA3	Page 216

6.7.24 Other SFR Registers

Table 70. Other SFR Registers

Address	Register Name	Short Name	Details
0xD0	Program Status Word	PSW	Page 216

6.8 Device Register Details

Unspecified fields in the registers below must be written as zero and can be ignored on read. The mode column shows the access for the field:

R/W Both read and write

R/O Read only

W/O Write only (read dummy)

6.8.1 System Block Registers (Block 7)

The following section lists the registers for the system block.

Table 71. CPU Transfer Mode—CPUMODE (Address 0x00)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
3	ENDIAN	R/W	Configures the byte order mode on SI and PI (if present) interfaces. 0: For SI, least significant byte first. For PI, least significant byte first (A0=0). 1: For SI, most significant byte first. For PI, most significant byte first.	0x1
0	BITDONE	R/W	Configures the SI and PI (if present) interfaces as: 0: For SI, least significant bit first in each byte. For PI, PI_nDone active high 1: For SI, most significant bit first in each byte. For PI, PI_nDone active low.	0x1
If the ICPU_PI_En strapping pin is strapped high, the parallel interface is not present. The register controls the data transfer mode for the CPU interfaces. For the write to work independently of the current transfer mode, BITDONE must be mirrored to bits 7, 8, 15, 16, 23, 24, and 31; and ENDIAN must be mirrored to bit 4, 11, 12, 19, 20, 27, and 28. In this respect, the possible values for this register are: 0x00000000 Little endian, least significant bit first / PI_nDone active high 0x18181818 Big endian, least significant bit first / PI_nDone active high 0x81818181 Little endian, most significant bit first / PI_nDone active low 0x99999999 Big endian, most significant bit first / PI_nDone active low.				

Table 72. SI Padding—SIPAD (Address 0x01)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
2:0	SIPAD	R/W	Cycle count.	0x2
Number of byte cycles (0-7) during SI read between command and the first byte read. Used to assure 200-ns delay and must be set according to the SI clock frequency.				

Table 73. PI Config—PICONF (Address 0x02)
Block 7 Subblock0

Bit	Name	Mode	Description	Default
3	AUTO_A1	W/O	Address line 1 is not sensed. In 8-bit bus mode, A1 is assumed to be zero in the first two accesses.	0x0
2	AUTO_A0	W/O	Address line 0 is not sensed. In 8-bit bus mode, A0 is assumed to be zero in the first access.	0x0
A single 8-bit write to this register is effective.				

Table 74. GMII Clock Delay—GMIIDELAY (Address 0x05)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
5:4	GMII0_GTXDELAY	R/W	Specifies delay on GMII0_GTx_Clk after output data. 00: No delay. 01: Delay is 1.4 ns. 10: Delay is 1.7 ns. 11: Delay is 2.0 ns.	0x0
1:0	GMII0_RXDELAY	R/W	Specifies delay on GMII0_Rx_Clk before input sampling. 00: No delay. 01: Delay is 1.4 ns. 10: Delay is 1.7 ns. 11: Delay is 2.0 ns.	0x0
Note The recommended value for RGMII mode is 11. When 11 is used, no external routing delay is required. The recommended value for GMII/MII mode is 00, with INVERT_GTX set in ADVPORTM. This provides maximum setup and hold.				

Table 75. Semaphore Register—HWSEM (Address 0x13)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
0	SEMAPHORE	R/W	This field behaves like a semaphore. Read this field to take the semaphore. If the read returns 1, the semaphore-reader has the semaphore. If the read returns 0, the semaphore-reader must continue to read the register. To release the semaphore, the semaphore-owner must write a 1 to this field.	0x0

Table 76. Global Reset—GLORESET (Address 0x14)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
4	STROBE	W/O	Used to enable access to the xxx_LOCK fields. For example, write 0x14 to this register to lock the memory initialization. Perform a soft-reset in two steps: first write to the lock-bits to prevent the internal CPU or the memories from being reset; then write to the MASTER_RESET bit to perform the reset.	0x0
3	ICPU_LOCK	R/W	Used to prevent the internal CPU from being reset when MASTER_RESET is asserted.	0x0
2	MEM_LOCK	R/W	Used to prevent the internal memory initialization from being reset when MASTER_RESET is asserted. If this bit is 0 during a MASTER_RESET, the memory initialization *must* be rerun to ensure proper operation of the switch. For more information about the internal memory initialization, see "Minimum Software Requirements," page 139.	0x0
1	PHY_RESET	R/W	Write 1 for releasing reset to the internal PHYs.	0x0
0	MASTER_RESET	W/O	Write 1 to this register to execute software reset. The reset acts as an external reset except that the protected registers are untouched if their corresponding lock signal is asserted. The reset should be followed by a delay of 125 µs before any access is made to the device. Do not write a 1 to this bit while also asserting the STROBE.	0x0

Table 77. Chip Identification—CHIPID (Address 0x18)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:28	REVISION_NUMBER	R/O	Revision ID: 0000: First revision 0001: Second revision ...	0x2
27:12	PART_NUMBER	R/O	BCD Encoded Part Number for this device.	0x7395
11:1	MANUFACTURER_ID	R/O	The unique identifier for the device vendor.	0x074
0	RESERVED	R/O	Always read as 1.	0x1
This register returns the same value as the JTAG Identifier.				

Table 78. Time Compare Value—TIMECMP (Address 0x24)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
25:0	TIMECMP	R/W	Time value for frame age calculation.	0x3B9ACA0
Sets the time determining how long a frame can be queued in SparX-G5e before it is regarded as being too old and dropped. Aging occurs after 25.6 ns times the value of this register. Default value equals 1.6 seconds. Setting TIMECMP to zero effectively disables aging. Requires that ports are reset (for example, setting MAC_CFG bits 29 (PORT_RST), 5 (MAC_RX_RST) and 4 (MAC_TX_RST)).				

Table 79. SlowData—SLOWDATA (Address 0x2C)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:0	SLOWDATA	R/O	This is the read data from slow registers.	0x00000000
When read, the SlowDone bit in the SYSTEM::CPUCTRL register is cleared. This register is only present when the parallel interface is enabled.				

Table 80. CPU Control—CPUCTRL (Address 0x30)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
11:8	PI_WAIT	R/W	Number of clock cycles to wait after PI_nCS is seen as low before other inputs are sampled. The unit is 12.8 ns, thereby allowing the input signals to be unstable for up to 192 ns more than the datasheet specifies. The field should be lowered to match the performance that the PI master can deliver. The value of this field is only used when the parallel interface is enabled.	0xF
5	EXT_CPU_USE_SLOW	R/W	Use slow mode for slow registers when accessed through PI, splitting a read operation into two phases. The value of this field is only used when the parallel interface is enabled.	0x0
4	SLOW_DONE	R/O	Set when a slow register operation is complete internally. Cleared when the SLOWDATA register is read or when a new slow data operation is initiated. The value of this field is only valid when the parallel interface is enabled.	0x0
3	INVERSE_IRQ1_POLARITY	R/W	Set the PI_IRQ1 interrupt signal to be active low. This field is only used when the parallel interface is enabled.	0x0
2	INVERSE_IRQ0_POLARITY	R/W	Set the PI_IRQ0 interrupt signal to be active low. This field is only used when the parallel interface is enabled.	0x0
1	IRQ1_ENABLE_SLOW	R/W	Enables interrupt on PI_IRQ1 when a slow register read or write is complete. This field is only used when the parallel interface is enabled.	0x0
0	IRQ0_ENABLE_SLOW	R/W	Enables interrupt on PI_IRQ0 when a slow register read or write is complete. This field is only used when the parallel interface is enabled.	0x0

Table 81. Capture Control—CAPCTRL (Address 0x31)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31	QUEUE1_READY	R/O	Captured frames are ready in queue 1.	0x0
30	QUEUE0_READY	R/O	Captured frames are ready in queue 0.	0x0
18	ARPBC_Q	R/W	Select the queue to which ARP broadcasts are captured.	0x0
17	IPMC_Q	R/W	Select the queue to which IPMC Control packets are captured.	0x0
16	IGMP_Q	R/W	Select the queue to which IGMP packets are captured.	0x0
15	ALLBRIDGE_Q	R/W	Select the queue to which ALLBRIDGE packets are captured.	0x0
14	GARP_Q	R/W	Select the queue to which GARP packets are captured.	0x0
13	BPDU_Q	R/W	Select the queue to which BPDU packets are captured.	0x0
12	FIFO_MODE	R/W	When set, frames are read from the capture RAM using only offset zero. When cleared, the capture RAM is accessed on successive addresses.	0x0
10:7	QUEUE1_MEM	R/W	Number of kilobytes reserved for queue 1. Queue 0 is allocated the rest of the 16-kilobyte capture memory.	0x0
6	Q1_IRQ_EN	R/W	Enable interrupt when queue 1 is non empty.	0x0
5	Q0_IRQ_EN	R/W	Enable interrupt when queue 0 is non empty.	0x0
4	Q1_IRQ_PIN	R/W	Select IRQ1 or IRQ0 for queue 1 interrupts. 0: Use PI_IRQ0 pin for signaling queue 1 ready. 1: Use PI_IRQ1 pin for signaling queue 1 ready.	0x0
3	Q0_IRQ_PIN	R/W	Select IRQ1 or IRQ0 for queue 0 interrupts. 0: Use PI_IRQ0 pin for signaling queue 0 ready. 1: Use PI_IRQ1 pin for signaling queue 0 ready.	0x0
2	LEARN_TRUNCATE	R/W	Captured frames for learning are truncated to 64 bytes.	0x0
1	LEARN_Q	R/W	Select the queue to which learn packets are captured.	0x0
0	MACB_Q	R/W	Select the queue to which MAC/VLAN-based frames are captured.	0x0

Table 82. General-Purpose I/O—GPIO (Address 0x34)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
7	OUTPUT_ENABLE_3	R/W	GPIO3 is an output type.	0x0
6	OUTPUT_ENABLE_2	R/W	GPIO2 is an output type.	0x0
5	OUTPUT_ENABLE_1	R/W	GPIO1 is an output type.	0x0
4	OUTPUT_ENABLE_0	R/W	GPIO0 is an output type.	0x0
3	DATA_VALUE_3	R/W	The value seen on the GPIO3 pins when read, and the value to output when written.	0x1

Table 82. General-Purpose I/O—GPIO (Address 0x34) *(continued)*
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
2	DATA_VALUE_2	R/W	The value seen on the GPIO2 pins when read, and the value to output when written.	0x1
1	DATA_VALUE_1	R/W	The value seen on the GPIO1 pins when read, and the value to output when written.	0x1
0	DATA_VALUE_0	R/W	The value seen on the GPIO0 pins when read, and the value to output when written.	0x1
When the GPIO pins are set into output mode, the value read matches the value written.				

Table 83. SI Master Interface—SIMASTER (Address 0x35)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
5	CHKSUM_ERR	R/W	Sticky bit for check sum error indicator. The bit is cleared by writing a 1 to it.	0x0
4	SI_DI	R/O	Current level on SI_Di pin.	0x0
3	MASTER	R/W	SI_Do, SI_nEn and SI_Clk are output enabled when this field is set.	0x0
2	SI_CLK	R/W	Set level of the SI_Clk pin.	0x0
1	SI_NEN	R/W	Set level of the SI_nEn pin.	0x0
0	SI_DO	R/W	Set level of the SI_DO pin.	0x0

6.8.2 V-Core CPU Block Registers (Block 7)

The following section lists the registers for the V-Core CPU block.

Table 84. Internal CPU Control—ICPU_CTRL (Address 0x10)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31	WATCHDOG_RST	R/W	This bit gets set by the hardware if the ICPU is reset due to failure in servicing the watchdog in due time. Write a 1 to clear it.	0x0
12:8	CLK_DIV	R/W	Selects the ICPU's clock frequency. The resulting frequency is computed as 156.25 MHz / (CLK_DIV + 1). Upon a system reset, the frequency is 156.25 MHz / 32 or approximately 4.88 MHz. The SparX-G5e device ignores writes of zero to this field.	0x1F
7	SOFT_RST_HOLD	R/W	Normally the SOFT_RST bit in this register is auto-released. By setting SOFT_RST_HOLD together with clearing SOFT_RST, the V-Core CPU is kept in the reset state until this bit is cleared again. When SOFT_RST is 1, the value of this bit has no influence.	0x0
6	ICPU_PI_En	R/O	Returns the value of the ICPU_PI_En strapping pin. 0: The V-Core CPU does not have access to the PI. 1: The V-Core CPU has access to the PI. The normal purpose of the PI is disabled.	0x1
3	BOOT_EN	R/W	Setting this bit causes the on-chip RAM to be mapped into address 0x0 in program memory space. By default, this bit is cleared, effectively making an external flash mapped into address 0x0 of the code space. Care should be taken not to execute code currently running in the lower eight kilobytes of the flash while setting this bit. A sound way to use this bit is in conjunction with the SOFT_RST bit (see SOFT_RST bit in this register). Setting both bits simultaneously causes the ICPU to reboot from on-chip RAM. This bit is a mirror of the ICPU_ROM_MAP::MAP_0 bit.	0x0
2	EXT_ACC_EN	R/W	This field is intended for debugging purposes only. It enables external access to both the on-chip scratchpad and eight-kilobyte CRAM/DRAM. The on-chip CPU should be stopped or held in the reset state, while an external CPU manipulates the contents of the RAM(s). Two registers, ICPU_ADDR and ICPU_DATA, provide read/write access to the RAMs after EXT_ACC_EN is enabled.	0x0
1	CLK_EN	R/W	When this bit is 1, the ICPU's clock is running; when 0, it's stopped. When debugging the on-chip scratchpad and/or CRAM/DRAM RAMs, the ICPU must be halted using this control bit or held in the reset state using the SOFT_RST control bit. **Note** Be sure to have the ICPU's watchdog disabled when disabling the ICPU's clock, because the watchdog is active even when the ICPU is sleeping.	0x1

Table 84. Internal CPU Control—ICPU_CTRL (Address 0x10) *(continued)*
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
0	SOFT_RST	R/W	Write a 0 to this bit to soft-reset the ICPU. Upon reset, the ICPU starts executing instructions from the code memory space's address 0x0000. When the ICPU is running, this bit always returns 1. See also the SYSTEM::GLORESET register for a description of how to reset the SparX-G5e device without resetting the V-Core CPU.	0x1

Table 85. Internal CPU On-Chip RAM Address—ICPU_ADDR (Address 0x11)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31	SP_SELECT	R/W	Scratchpad RAM select.If cleared, the 8-kilobyte RAM is accessed by this register and the ICPU_DATA register. If set, the 256-byte scratchpad RAM is accessed by this register and the ICPU_DATA register.	0x0
12:0	ADDR	R/W	Sets the access address of the on-chip RAMs. Only the eight least significant bits are used when SP_SELECT is 1.	0x0000
This register is intended for debugging purposes only.				

Table 86. Internal CPU On-Chip RAM Data—ICPU_DATA (Address 0x12)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
7:0	DATA	R/W	Read or write this field to get or set the data held in the selected RAM's address pointed to by the ICPU_ADDR::ADDR field. The address is auto-incremented after the access. The ICPU_CTRL register's EXT_ACC_EN field must be set to 1 prior to accessing this register. If not, reading or writing this register has no effect other than incrementing the ICPU_ADDR register, which wraps around from 0x1FFF to 0x0000 independent of the SP_SELECT value.	0x00
This register is intended for debugging purposes only.				

Table 87. Mailbox Value—ICPU_MBOX_VAL (Address 0x15)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:0	MBOX_VAL	R/O	Read this register to obtain the current value of the mailbox used for exchanging data or events between the internal and an external CPU. Its value is changed by the use of the ICPU_MBOX_SET and ICPU_MBOX_CLR registers. It is suggested that the 32 bits are split into two or more segments, so that events can be signaled from the internal to the external CPU through one segment and vice versa. For example, the ICPU_MBOX_SET register is used by the ICPU on segment number 1 only, and the ICPU_MBOX_CLR is used by the ICPU on segment number 2, only, and vice versa. The semaphore register, HWSEM, may be used to protect shared bits, which can be allocated in a third segment of this register.	0x00000000
The register is general purpose and may be used without the V-Core CPU being enabled.				

Table 88. Mailbox Set—ICPU_MBOX_SET (Address 0x16)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:0	MBOX_SET	W/O	Write this register to set the corresponding bits in ICPU_MBOX_VAL. Only bits that are 1 are set in the ICPU_MBOX_VAL register; the remaining are untouched.	0x00000000
The register is general purpose and may be used without the V-Core CPU being enabled.				

Table 89. Mailbox Clear—ICPU_MBOX_CLR (Address 0x17)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
31:0	MBOX_CLR	W/O	Write this register to clear the corresponding bits in ICPU_MBOX_VAL. Only bits that are 1 are cleared in the ICPU_MBOX_VAL register; the remaining are untouched.	0x00000000
The register is general purpose and may be used without the V-Core CPU being enabled.				

Table 90. External Data Memory Access Control Configuration—ICPU_RAM_CFG (Address 0x19)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
18:16	CHIP_SEL_WRITE_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the RAM Chip Select signal (ICPU_RAM_nCS) for data writes (ICPU_nWR active).	0x2

Table 90. External Data Memory Access Control Configuration—ICPU_RAM_CFG (Address 0x19) *(continued)*

Bit	Name	Mode	Description	Default
14:12	CHIP_SEL_READ_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the RAM Chip Select signal (ICPU_RAM_nCS) for data reads (ICPU_nRD active).	0x1
10:8	WRITE_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the write enable signal (ICPU_nWR) for data writes.	0x2
6:4	READ_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the read enable signal (ICPU_nRD) for data reads.	0x1
2:0	WRITE_DATA_HOLD	R/W	Controls the number of 6.4 ns cycles that the ICPU holds written data (ICPU_Data[7:0]) beyond normal.	0x3
The value written to this register has no effect unless the ICPU_PI_En strapping pin is strapped high.				

Table 91. External Program Memory Access Control Config.—ICPU_ROM_CFG (Address 0x1A)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
18:16	CHIP_SEL_WRITE_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the Chip Select signal (ICPU_ROM_nCS) for instruction writes (ICPU_nWR active).	0x2
14:12	CHIP_SEL_READ_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the Chip Select signal (ICPU_ROM_nCS) for instruction reads (ICPU_nRD active).	0x1
10:8	WRITE_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the write enable signal (ICPU_nWR) for instruction writes.	0x2
6:4	READ_DELAY	R/W	Controls the number of 6.4 ns cycles that the ICPU delays the read enable signal (ICPU_nRD) for instruction reads.	0x1
2:0	WRITE_DATA_HOLD	R/W	Controls the number of 6.4 ns cycles that the ICPU holds written instruction data (ICPU_Data[7:0]) beyond normal.	0x3
The value written to this register has no effect unless the ICPU_PI_En strapping pin is strapped high.				

Table 92. On-Chip RAM Mapping in Data Memory Space—ICPU_RAM_MAP (Address 0x1B)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
7	MAP_7	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0xE000-0xFFFF.	0x1
6	MAP_6	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0xC000-0xCFFF.	0x0
5	MAP_5	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0xA000-0xBFFF.	0x0

Table 92. On-Chip RAM Mapping in Data Memory Space—ICPU_RAM_MAP (Address 0x1B) *(continued)*

Bit	Name	Mode	Description	Default
4	MAP_4	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0x8000-0x9FFF.	0x0
3	MAP_3	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0x6000-0x7FFF.	0x0
2	MAP_2	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0x4000-0x5FFF.	0x0
1	MAP_1	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0x2000-0x3FFF.	0x0
0	MAP_0	R/W	Set this bit to map the 8-kilobyte on-chip RAM into data memory space addresses 0x0000-0x1FFF.	0x0
The value written to this register has no effect unless the ICPU_PI_En strapping pin is strapped high.				

Table 93. On-Chip RAM Mapping in Code Memory Space—ICPU_ROM_MAP (Address 0x1C)
Block 7 Subblock 0

Bit	Name	Mode	Description	Default
7	MAP_7	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0xE000-0xFFFF.	0x1
6	MAP_6	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0xC000-0xCFFF.	0x0
5	MAP_5	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0xA000-0xBFFF.	0x0
4	MAP_4	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0x8000-0x9FFF.	0x0
3	MAP_3	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0x6000-0x7FFF.	0x0
2	MAP_2	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0x4000-0x5FFF.	0x0
1	MAP_1	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0x2000-0x3FFF.	0x0
0	MAP_0	R/W	Set this bit to map the 8-kilobyte on-chip RAM into code memory space addresses 0x0000-0x1FFF. This bit is mirrored into ICPU_CTRL::BOOT_EN.	0x0
The value written to this register has no effect unless the ICPU_PI_En strapping pin is strapped high. In addition, all code memory writes are always forwarded to the external interface independently of setting of these bits.				

6.8.3 PORTREG Block Registers (Block 1)

For writing the same register in all devices, use virtual device 31. This is mapped to block 6, subblock 15. Only the devices that are enabled (default value) for this register perform an update. The devices can be configured in the ALLMEMBER register.

Table 94. Device Register Mode—REGMODE (Address 0x01)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
0	ALLMEMBER	R/W	Set to 1 if the write to device 31 (all ports) must be executed by this specific port.	0x1

6.8.4 MAC Block Registers (Block 1)

The following section lists the registers for the MAC block.

Table 95. MAC Configuration—MAC_CFG (Address 0x00)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
31	WEXC_DIS	R/W	Determines whether or not the MAC backs off after an excessive collision has occurred. If set, backoff is disabled after excessive collisions.	0x0
29	PORT_RST	R/W	The port is held reset while this bit is set. Only the shared FIFO block registers are reset. All other port configurations are kept.	0x1
28	TX_EN	R/W	Enable frame transmission.	0x0
27	SEED_LOAD	R/W	Load seed for backoff algorithm.	0x0
26:19	SEED	R/W	Value used to seed the randomizer used for the backoff algorithm. To load a seed into the randomizer, a transmit clock must be present, and the transmitter must be idle. The SEED_LOAD must be asserted for at least 1 µs, and the SEED field must not be changed simultaneously with deassertion of SEED_LOAD.	0x00
18	FDX	R/W	Enable full-duplex mode.	0x1
17	GIGA_MODE	R/W	Set MAC to gigabit mode.	0x0
16	RX_EN	R/W	Enable receiver.	0x0
15	VLAN_DBLAWR	R/W	Allow double tagged frames to be MAXLEN::MAX_LENGTH + 8 bytes long.	0x0
14	VLAN_AWR	R/W	Allow tagged frames to be MAXLEN::MAX_LENGTH + 4 bytes long.	0x0
10:6	TX_IPG	R/W	The inter-frame gap between two consecutive transmitted frames. Recommended: 10/100: 17 1G: 6	0x00
5	MAC_RX_RST	R/W	The receive domain is held reset while this bit is set.	0x1

Table 95. MAC Configuration—MAC_CFG (Address 0x00) *(continued)*
Block 1 Subblock 0-4, 6

<table>
<tr><th>Bit</th><th>Name</th><th>Mode</th><th>Description</th><th>Default</th></tr>
<tr><td>4</td><td>MAC_TX_RST</td><td>R/W</td><td>The transmit domain is held reset while this bit is set.</td><td>0x1</td></tr>
<tr><td>2:0</td><td>CLK_SEL</td><td>R/W</td><td>Clock selection. The following table illustrates which settings can be used for specific PHY interfaces.
Note For more information about the MII connection to external MAC, see “Reverse MII,” page 283,
<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="5">PHY Interface</th></tr>
<tr><th>Internal PHY</th><th>GMII/MII</th><th>RGMII</th><th>Reverse MII</th><th>Not used</th></tr>
<tr><td rowspan="5">CLK_SEL Settings</td><td>000</td><td></td><td></td><td></td><td></td><td>X</td></tr>
<tr><td>001</td><td></td><td>GMII (1 Gbps)</td><td>125 MHz (1 Gbps)</td><td></td><td></td></tr>
<tr><td>010</td><td></td><td></td><td>25 MHz (100 Mbps)</td><td>100 Mbps</td><td></td></tr>
<tr><td>011</td><td></td><td></td><td>2.5 MHz (10 Mbps)</td><td>10 Mbps</td><td></td></tr>
<tr><td>100</td><td>X</td><td>MII (100 Mbps/ 10 Mbps) (uses external clock)</td><td></td><td></td><td></td></tr>
</table></td><td>0x0</td></tr>
<tr><td colspan="5">This register configures most MAC functions. When changing the clock or duplex select fields, the register must be written twice: once with all three reset flags asserted, once without.</td></tr>
</table>

Table 96. Half-Duplex Gaps—MACHDXGAP (Address 0x02)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
19:16	RESERVED	R/W	Must be default value.	0x7
15:12	BACKOFFBIAS	R/W	This value can be used to adjust the backoff time with a resolution of 8-bit times. If the register is increased by 1, the backoff time is decreased by 8-bit times. The correct value depends on the delay from the MAC to the I/O pads and should normally be set to its default value.	0x8
11:8	LCOLPOS	R/W	Late Collision Position. Adjust the border between a collision and a late collision in steps of 1 byte. According to IEEE Std 802.3 section 21.3 this border is allowed to be on data byte 56 (counting frame data from 1), that is, a frame experiencing a collision on data byte 55 is always retransmitted, and on byte 57, it is never retransmitted. Using LCOLPOS = 2, the border is in this range. For each higher LCOLPOS value, the border is moved 1 byte higher.	0x2
7:4	IFG2	R/W	Second part of half-duplex Rx to Tx inter-frame gap. Within IFG2, transitions on CRS are ignored.	0x8

Table 96. Half-Duplex Gaps—MACHDXGAP (Address 0x02) *(continued)*
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
3:0	IFG1	R/W	First part of half-duplex Rx to Tx inter-frame gap. The sum of IFG1 and IFG2 times the Rx to Tx IFG. Within IFG1, this timing is restarted if CRS has multiple high-low transitions, that is, is noisy.	0x6

Table 97. Flow Control Setup—FCCONF (Address 0x04)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
17	ZERO_PAUSE_EN	R/W	If set, a zero delay pause frame is transmitted when pause condition is left.	0x0
16	FLOW_CTRL_OBEY	R/W	Obey pause control frames.	0x0
15:0	PAUSE_VAL	R/W	This value is inserted into the generated pause frames.	0x0000
This register controls the flow control setup. The frames are generated by the conditions set up in Q_MISC_CONF.				

Table 98. Flow Control SMAC High—FCMACHI (Address 0x08)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	FCMACHI	R/W	These are the upper three bytes inserted in the generated flow control frames.	0x000000

Table 99. Flow Control SMAC Low—FCMACLO (Address 0x0C)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	FCMACLO	R/W	These are the lower three bytes inserted in the generated flow control frames.	0x000000

Table 100. Maximum Length—MAXLEN (Address 0x10)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
16	TYPE_LEN_CHECK	R/W	Enable check of valid type/length field. If enabled, ingress frames can be dropped due to inrange or outrange errors.	0x0
15:0	MAX_LENGTH	R/W	Frame is long and dropped if frame length exceeds this limit. The internal limit is 9.6 kilobytes. For information about tagged and double-tagged frame length check, see bits VLAN_AWR and VLAN_DBLAWR in Table 95, page 161	0x05EE

Table 101. Advanced Port Mode Setup—ADVPORTM (Address 0x19)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
7	IFG_PPM	R/W	Auto-reduce egress IFG by one byte when PPM differences are present.	0x0
6	EXC_COL_CONT	R/W	If set, a frame is not discarded after 16 collisions. However, the backoff algorithm is restarted.	0x0
5	EXTERNAL_PORT	R/W	Select external interface for this port, when set to 1.	0x0
4	INVERT_GTX	R/W	If set, the GMII GTX external clock is inverted.	0x0
3	ENABLE_GTX	R/W	If set, the GMII GTX external clock is activated.	0x0
2	DDR_MODE	R/W	If set, the interface runs double data rate.	0x0
1	IO_LOOPBACK	R/W	If set, all Rx data is echoed to the Tx pins.	0x0
0	HOST_LOOPBACK	R/W	If set, all Tx data is echoed to the ingress path.	0x0

Table 102. Tx Queue Selector Configuration—TXQ_SELECT_CFG (Address 0x28)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
31	WEIGHTED_PRIO_ENA	R/W	Enables use of the round-robin table for weighted priority. Otherwise, strict priority is used.	0x0
30	REDUCED_ENA	R/W	Enables use of reduced table where on the first eight slots are used. The is for example convenient when equal rates must to be configured.	0x0
19:18	SLOT9	R/W	QoS class for round-robin slot 9.	0x0
17:16	SLOT8	R/W	QoS class for round-robin slot 8.	0x0
15:14	SLOT7	R/W	QoS class for round-robin slot 7.	0x0
13:12	SLOT6	R/W	QoS class for round-robin slot 6.	0x0
11:10	SLOT5	R/W	QoS class for round-robin slot 5.	0x0
9:8	SLOT4	R/W	QoS class for round-robin slot 4.	0x0
7:6	SLOT3	R/W	QoS class for round-robin slot 3.	0x0
5:4	SLOT2	R/W	QoS class for round-robin slot 2.	0x0
3:2	SLOT1	R/W	QoS class for round-robin slot 1.	0x0
1:0	SLOT0	R/W	QoS class for round-robin slot 0.	0x0
This register controls the Tx queue selection process. If WEIGHTED_PRIO_ENA is set, the SLOT0 through SLOT9 are cycled through in a round-robin fashion and control which QoS class gets the next transmission slot. If WEIGHTED_PRIO_ENA is cleared, the selection is strict priority.				

Table 103. Transmit Modify Setup—TXUPDCFG (Address 0x24)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
20:19	DSCP_REWR_MODE	R/W	Set mode for IPv4 and IPv6 DSCP rewrite. Encoding: 00: Map QoS Class to AF CPs: 0: 001100 (AF12) 1: 010100 (AF22) 2: 011100 (AF32) 3: 100100 (AF42) 01: Map QoS Class to Class Selector CPs: 0: 000000 1: 001000 2: 010000 3: 011000 10: Remap QoS Class and then map to AF CPs. Same as 00, but QoS Class is now first remapped using CAT_GENERIC_PRIO_REMAP and remapped value is then used to map to AF CP. 11: Remap QoS Class and then map to CS CP. Same as 01, but QoS Class is now first remapped using CAT_GENERIC_PRIO_REMAP and remapped value is then used to map to Class Selector CP.	0x0
18	DSCP_REWR_ENA	R/W	Enable rewrite of DSCP in outgoing IPv4 and IPv6 packets provided ingress port marked the frame for DSCP rewrite. The actual value to be written is controlled by DSCP_REWR_MODE. See also related fields in CAT_PR_MISC_L3 (Table 117).	0x0
17	TX_INT_TO_USRPRIO_ENA	R/W	Map QoS Class to tag priority using CAT_GENERIC_PRIO_REMAP.	0x0
15:4	TX_UNTAGGED_VID	R/W	Frames with this VID are transmitted untagged.	0x000
3	TX_UNTAGGED_VID_ENA	R/W	If set, frames with VID=TX_UNTAGGED_VID are not tagged, even if port is set up for tagging.	0x0
1	TX_UPDATE_CRC_CPU_ ENA	R/W	Recalculate CRC for all frames from CPU.	0x0
0	TX_INSERT_TAG	R/W	If set, frames are transmitted with VLAN tags. Exceptions to this can be configured in TX_UNTAGGED_VID_ENA.	0x0

6.8.5 Shared FIFO Block Registers (Block 1)

The following section lists the shared FIFO block registers.

Table 104. CPU Transmit DATA—CPUTXDAT (Address 0xC0)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
31:0	CPUTXDAT	W/O	Write four bytes of Tx Data. An even number of writes *must* be performed.	0x00000000
This register is used by the CPU to transmit frames. The first two words must hold a header for the frame, which is: word1: The length shifted left by 16 bits. word2: 0x00000520.				

Table 105. Miscellaneous Control Register—MISCFIFO (Address 0xC4)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
1	REWIND_CPU_TX	W/O	Cancel the CPU Tx Data that has been through the CPUTXDAT register.	0x0
0	CPU_TX	W/O	Transmit the frame data written through the Transmit Data register.	0x0
This register can only be written when the port is activated through MAC_CFG::PORT_RST.				

Table 106. Miscellaneous Status—MISCSTAT (Address 0xC8)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
8	CPU_TX_DATA_PENDING	R/O	Indicates that Tx data recently written to CPUTXDAT was not yet transferred to the Tx queue. No further writes to CPUTXDAT must take place before this bit is clear.	0x0
7	CPU_TX_DATA_OVERFLOW	R/O	Indicates that additional Tx data was written by the CPU before the CPU_TX_DATA_PENDING bit was cleared. When this flag is detected, the rewind command must be issued.	0x0

Table 107. Free RAM Counter—FREEPOOL (Address 0xD8)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
21:16	FREE_CNT	R/O	Minimum number of free 512-byte slices of RAM in shared FIFO since last read.	0x27
13:8	INGR_USED	R/O	Maximum number of 512-byte slices used for ingress data since last read.	0x00

Table 107. Free RAM Counter—FREEPOOL (Address 0xD8) *(continued)*
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
5:0	EGR_USED	R/O	Maximum number of 512-byte slices used for egress data since last read.	0x00

Table 108. Flow Control Watermarks—Q_FLOWC_WM (Address 0xDE)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
13:8	FWDP_START	R/W	Stop ingress enqueuing when amount of ingress data exceeds this slice count.	0x1F
5:0	FWDP_STOP	R/W	Resume ingress enqueuing when amount of ingress data falls below this slice count (hysteresis condition).	0x1F
1 slice = 512 bytes				

Table 109. Miscellaneous Pool Control—Q_MISC_CONF (Address 0xDF)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
31	EXTENT_MEM	R/W	Set to enable 20-kilobyte buffer. Otherwise, 16-kilobyte buffer is used.	0x0
4:1	EARLY_TX		Allow early initiation of MAC transmission if the amount of egress data is below the EARLY_TX value times 512 bytes.	0x0
0	MAC_PAUSE_MODE	R/W	Select which method to use when avoiding ingress overflow as determined by the FWDP_START and FWDP_STOP watermarks. When this field is set, pause control frames are issued. Default value (0) makes the ingress queue forwarding disobey egress back pressure.	0x0
Note The early transmission level is used for jumbo frame support. For more information about jumbo frame support, contact your Vitesse representative.				

Table 110. Drop Watermarks—Q_DROP_WM (Addresses 0xE0-0xE3)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
29:24	EGRESS_MIN	R/W	Do not drop egress frames when the amount of egress data for this queue falls below this number of slices.	0x00
21:16	EGRESS_MAX	R/W	Drop egress frames when the amount of egress data exceeds this number of slices.	0x1F
13:8	INGRESS_MIN	R/W	Do not drop ingress frames when the amount of ingress data for this queue falls below this number of slices.	0x00

Table 110. Drop Watermarks—Q_DROP_WM (Addresses 0xE0-0xE3) *(continued)*
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
5:0	INGRESS_MAX	R/W	Drop ingress frames when the amount of ingress data exceeds this number of slices.	0x1F
A drop watermark register exists for each drop class. Note that both the check against total consumption for the direction (MAX watermarks), as well as the queue-specific check (MIN watermarks) must result in drop for a frame to get discarded. 1 slice = 512 bytes.				

6.8.6 Categorizer Block Registers (Block 1)

The categorizer performs the following frame-processing tasks:

- Determines whether frame should be dropped due to illegal MAC address.
- Determines whether frame should be forwarded to the CPU.
- Determines the QoS class for the frame.
- Determines VID for the frame.
- Generates aggregation code for frame.
- Controls whether DSCP in IPv4 and IPv6 packets should be rewritten on egress.
- Controls whether any incoming tag header should be removed from the frame.

Table 111. Categorizer Frame Dropping—CAT_DROP (Address 0x6E)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
6	DROP_MC_SMAC_ENA	R/W	Drop frames with multicast source MAC address.	0x0
4	FWD_CTRL_ENA	R/W	Forward MAC control frames.	0x0
3	FWD_PAUSE_ENA	R/W	Forward pause frames.	0x0
2	DROP_UNTAGGED_ENA	R/W	Drop untagged frames.	0x0
1	DROP_TAGGED_ENA	R/W	Drop tagged frames.	0x0
0	DROP_NULL_MAC_ENA	R/W	Drop frames with source or destination MAC address equal to 00-00-00-00-00-00.	0x1

Table 112. Categorizer Miscellaneous Layer-2 QoS—CAT_PR_MISC_L2 (Address 0x6F)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
28	USR_PRIO_ENA	R/W	Enable QoS class based on user priority.	0x0
18	CPU_HIGHQOS	R/W	Classify all packets potentially for the CPU as high priority.	0x1
17:16	PORT_QOS	R/W	Port-based QoS class.	0x3

Table 113. Categorizer User Priority—CAT_PR_USR_PRIO (Address 0x75)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
29:28	USR_PRIO7_QOS	R/W	QoS class for user priority = 7.	0x3
25:24	USR_PRIO6_QOS	R/W	QoS class for user priority = 6.	0x3
21:20	USR_PRIO5_QOS	R/W	QoS class for user priority = 5.	0x2
17:16	USR_PRIO4_QOS	R/W	QoS class for user priority = 4.	0x2
13:12	USR_PRIO3_QOS	R/W	QoS class for user priority = 3.	0x1
9:8	USR_PRIO2_QOS	R/W	QoS class for user priority = 2.	0x1
5:4	USR_PRIO1_QOS	R/W	QoS class for user priority = 1.	0x0
1:0	USR_PRIO0_QOS	R/W	QoS class for user priority = 0.	0x0
Use of user priority for determining QoS class is enabled by CAT_PR_MISC_L2::USR_PRIO_ENA.				

Table 114. Categorizer DSCP QoS—CAT_PR_DSCP_QOS (Address 0x60)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
29:28	DSCP_QOS_7	R/W	QoS class for other DSCP values.	0x0
25:24	DSCP_QOS_6	R/W	QoS class for corresponding DSCP value.	0x0
21:20	DSCP_QOS_5	R/W	QoS class for corresponding DSCP value.	0x0
17:16	DSCP_QOS_4	R/W	QoS class for corresponding DSCP value.	0x0
13:12	DSCP_QOS_3	R/W	QoS class for corresponding DSCP value.	0x0
9:8	DSCP_QOS_2	R/W	QoS class for corresponding DSCP value.	0x0
5:4	DSCP_QOS_1	R/W	QoS class for corresponding DSCP value.	0x0
1:0	DSCP_QOS_0	R/W	QoS class for corresponding DSCP value.	0x0
Use of IPv4/IPv6 DSCP for determining QoS class is enabled by CAT_PR_MISC_L3::DSCP_ENA.				

Table 115. Categorizer DSCP Values 0-3—CAT_PR_DSCP_VAL_0_3 (Address 0x61)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
29:24	DSCP_VAL_3	R/W	All frames with this DSCP value get QoS class DSCP_QOS_3.	0x00
21:16	DSCP_VAL_2	R/W	All frames with this DSCP value get QoS class DSCP_QOS_2.	0x00
13:8	DSCP_VAL_1	R/W	All frames with this DSCP value get QoS class DSCP_QOS_1.	0x00
5:0	DSCP_VAL_0	R/W	All frames with this DSCP value get QoS class DSCP_QOS_0.	0x00

Table 116. Categorizer DSCP Values 4-6—CAT_PR_DSCP_VAL_4_6 (Address 0x62)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
21:16	DSCP_VAL_6	R/W	All frames with this DSCP value get QoS class DSCP_QOS_6.	0x00
13:8	DSCP_VAL_5	R/W	All frames with this DSCP value get QoS class DSCP_QOS_5.	0x00
5:0	DSCP_VAL_4	R/W	All frames with this DSCP value get QoS class DSCP_QOS_4.	0x00

Table 117. Categorizer Miscellaneous Layer-3 QoS—CAT_PR_MISC_L3 (Address 0x77)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
28	DSCP_REWR_OTHER_ENA	R/W	If frame is IPv4 or IPv6 and DSCP is NOT any of the values covered by DSCP_REWR_ZERO_ENA, DSCP_REWR_CS_ENA, DSCP_REWR_AF_ENA or DSCP_REWR_EF_ENA, then mark the frame to have DSCP rewritten by the egress port. See also TXUPDCFG::DSCP_REWR_ENA and TXUPDCFG::DSCP_REWR_MODE (Table 103).	0x0
27	DSCP_REWR_ZERO_ENA	R/W	If frame is IPv4 or IPv6 and DSCP is zero, then mark the frame to have DSCP rewritten by the egress port. See also TXUPDCFG::DSCP_REWR_ENA and TXUPDCFG::DSCP_REWR_MODE (Table 103).	0x0
26	DSCP_REWR_CS_ENA	R/W	If frame is IPv4 or IPv6 and DSCP is one of the Class Selector CPs (see RFC2474) then mark the frame to have DSCP rewritten by the egress port. See also TXUPDCFG::DSCP_REWR_ENA and TXUPDCFG::DSCP_REWR_MODE (Table 103).	0x0
25	DSCP_REWR_AF_ENA	R/W	If frame is IPv4 or IPv6 and DSCP is one of the AF CPs (see RFC2597) then mark the frame to have DSCP rewritten by the egress port. See also TXUPDCFG::DSCP_REWR_ENA and TXUPDCFG::DSCP_REWR_MODE (Table 103).	0x0
24	DSCP_REWR_EF_ENA	R/W	If frame is IPv4 or IPv6 and DSCP is equal to the EF CP (see RFC3246) then mark the frame to have DSCP rewritten by the egress port. See also TXUPDCFG::DSCP_REWR_ENA and TXUPDCFG::DSCP_REWR_MODE (Table 103).	0x0
21	DSCP_ENA	R/W	Enable QoS class based on IPv4 or IPv6 DSCP.	0x0

Table 118. Categorizer VLAN Miscellaneous—CAT_VLAN_MISC (Address 0x79)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
8	VLAN_TCI_IGNORE_ENA	R/W	Ignore any tag header in received frame during VLAN classification. Any user-priority value in the tag header may still influence the priority classification, see CAT_PR_MISC_L2::USR_PRIO_ENA (Table 112).	0x1
7	VLAN_KEEP_TAG_ENA	R/W	Do not remove tag header from frame. If egress port tags frame, the resulting frame contains two tag headers.	0x1

Table 119. Categorizer Port VLAN—CAT_PORT_VLAN (Address 0x7A)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
15	VLAN_CFI	R/W	CFI value to use for port-based VLAN.	0x0
14:12	VLAN_USR_PRIO	R/W	User priority value to use for port-based VLAN.	0x0
11:0	VLAN_VID	R/W	VID value for port-based VLAN.	0x000

Table 120. Categorizer Other Configuration—CAT_OTHER_CFG (Address 0x7B)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
2	AC_IP6_FLOW_LBL_ENA	R/W	Use the 20 bits IPv6 Flow Label for aggregation code.	0x0
1	AC_SIPDIP_ENA	R/W	Use least significant eight bits of both SIP and DIP of IPv4 packets for aggregation code.	0x1
0	AC_TCPUDP_PORT_ENA	R/W	Use least significant eight bits of both SPORT and DPORT of IPv4 packets for aggregation code.	0x1

Table 121. Categorizer Generic Priority Remap—CAT_GENERIC_PRIO_REMAP (Address 0x7D)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
14:12	PRIO3	R/W	Remap value.	0x7
10:8	PRIO2	R/W	Remap value.	0x5
6:4	PRIO1	R/W	Remap value.	0x3
2:0	PRIO0	R/W	Remap value.	0x1
This register holds remapping table, which—depending on other configuration parameters—can be used for the following purposes: **1.** Map internal QoS class to user priority on egress, see TXUPDCFG::TX_INT_TO_USRPRIO_ENA (Table 103). **2.** Remap QoS class when rewriting DSCP on egress, see TXUPDCFG::DSCP_REWR_MODE (Table 103), encoding 10 and 11.				

6.8.7 Detailed Counters Block Registers (Block 1)

The counters in this block are for RMON-II counter support. They are cleared by writing the C_RX0 register with any value. All counters wrap around at their maximum values. For 1G operation, 24-bit counters can wrap around every 10 seconds whereas 32-bit counters can wrap around every 30 seconds depending on the traffic load. For 100-Mbps and 10-Mbps operations, these values must be scaled by a factor of 10 and 100, respectively.

Table 122. Rx Octets—C_RXOCT (Address 0x50)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
31:0	C_RXOCT	R/O	Received octets in good and bad packets.	0x00000000

Table 123. Tx Octets—C_TXOCT (Address 0x51)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
31:0	C_TXOCT	R/O	Transmitted octets in good and bad packets.	0x00000000

Table 124. Rx Counter 0—C_RX0 (Address 0x52)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	C_RX0	R/W	Counts per configuration in CNT_CTRL_CFG::CFG_RX0.	0x000000
Note that writing anything to this register clears all counters for the specific port.				

Table 125. Rx Counter 1—C_RX1 (Address 0x53)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	C_RX1	R/O	Counts per configuration in CNT_CTRL_CFG::CFG_RX1.	0x000000

Table 126. Rx Counter 2—C_RX2 (Address 0x54)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	C_RX2	R/O	Counts per configuration in CNT_CTRL_CFG::CFG_RX2.	0x000000

Table 127. Tx Counter 0—C_TX0 (Address 0x55)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	C_TX0	R/O	Counts per configuration in CNT_CTRL_CFG::CFG_TX0.	0x000000

Table 128. Tx Counter 1—C_TX1 (Address 0x56)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	C_TX1	R/O	Counts per configuration in CNT_CTRL_CFG::CFG_TX1.	0x000000

Table 129. Tx Counter 2—C_TX2 (Address 0x57)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
23:0	C_TX2	R/O	Counts per configuration in CNT_CTRL_CFG::CFG_TX2.	0x000000

Table 130. Counter Control Configuration—CNT_CTRL_CFG (Address 0x58)
Block 1 Subblock 0-4, 6

Bit	Name	Mode	Description	Default
30:26	CFG_TX2	R/W	Counter configuration of Tx counter 2.	0x02
25:21	CFG_TX1	R/W	Counter configuration of Tx counter 1.	0x01
20:16	CFG_TX0	R/W	Counter configuration of Tx counter 0.	0x00
14:10	CFG_RX2	R/W	Counter configuration of Rx counter 2.	0x02
9:5	CFG_RX1	R/W	Counter configuration of Rx counter 1.	0x01
4:0	CFG_RX0	R/W	Counter configuration of Rx counter 0.	0x00

The Tx and Rx counters have default values that can be configured for your application with any of the following values.

Table 131. Values for the Tx and Rx Counters in CNT_CTRL_CFG

TX or RX	Value	Counter Name	Counter Description
TX	0	Packets	Number of good and bad packets.
TX	1	Broadcasts+Multicasts	Number of good broadcasts and multicasts.
TX	2	Total error packets	Number of bad packets transmitted.
TX	3	Broadcasts	Number of good broadcasts.

Table 131. Values for the Tx and Rx Counters in CNT_CTRL_CFG *(continued)*

TX or RX	Value	Counter Name	Counter Description
TX	4	Multicasts	Number of good multicasts.
TX	5	64	Number of 64-byte frames in good and bad packets.
TX	6	65	Number of 65 to 127-byte frames in good and bad packets.
TX	7	128	Number of 128 to 255-byte frames in good and bad packets.
TX	8	256	Number of 256 to 511-byte frames in good and bad packets.
TX	9	512	Number of 512 to 1023-byte frames in good and bad packets.
TX	10	1024	Number of 1024 to 1526-byte frames in good and bad packets.
TX	11	Jumbo	Number of 1527-MAXLEN::MAX_LENGTH-byte frames in good and bad packets.
TX	12	Pause	Number of transmitted pause frames.
TX	13	FIFO drops	Number of frames dropped due to lack of transmit buffer.
TX	14	Drops	Number of frames dropped due to excessive collision, late collision or frame aging.
TX	15	Collisions	Number of collisions transmitting frames experience. An excessive collided frame gives 16 counts.
TX	16	CFI drop	Number of frames dropped due to CFI marking (CFI marked frames are dropped when the port is set up to transmit untagged frames).
TX	25	Total good packets	Number of good packets transmitted.
TX	26	Class0	Number of transmitted frames classified to QoS class 0.
TX	27	Class1	Number of transmitted frames classified to QoS class 1.
TX	28	Class2	Number of transmitted frames classified to QoS class 2.
TX	29	Class3	Number of transmitted frames classified to QoS class 3.
RX	0	Packets	Number of good and bad packets.
RX	1	Broadcasts+Multicasts	Number of good broadcasts and multicasts.
RX	2	Total error packets	Number of bad packets received.
RX	3	Broadcasts	Number of good broadcasts.
RX	4	Multicasts	Number of good multicasts.
RX	5	64	Number of 64-byte frames in good and bad packets.
RX	6	65	Number of 65 to 127-byte frames in good and bad packets.
RX	7	128	Number of 128 to 255-byte frames in good and bad packets.
RX	8	256	Number of 256 to 511-byte frames in good and bad packets.
RX	9	512	Number of 512 to 1023-byte frames in good and bad packets.
RX	10	1024	Number of 1024 to 1526-byte frames in good and bad packets.
RX	11	Jumbo	Number of 1527-MAXLEN::MAX_LENGTH-byte frames in good and bad packets.
RX	12	Pause	Number of received pause frames.
RX	13	FIFO drops	Number of frames dropped due to lack of receive buffer.
RX	14	Backward drops	Number of packets dropped due to egress congestion.

Table 131. Values for the Tx and Rx Counters in CNT_CTRL_CFG *(continued)*

TX or RX	Value	Counter Name	Counter Description
RX	15	Classifier drops	Number of packets dropped due to classifier rules.
RX	16	CRC	Number of CRC errors, Alignment errors and RX_ER events.
RX	17	Undersize	Number of short frames with valid CRC (<64 bytes).
RX	18	Oversize	Number of long frames with valid CRC (according to MAXLEN::MAX_LENGTH).
RX	19	Fragments	Number of short frames with invalid CRC (<64 bytes).
RX	20	Jabbers	Number of long frames with invalid CRC (according to MAXLEN::MAX_LENGTH).
RX	21	Control packets	Number of MAC control frames received.
RX	25	Total good packets	Number of good packets received.
RX	26	Class0	Number of received frames classified to QoS class 0.
RX	27	Class1	Number of received frames classified to QoS class 1.
RX	28	Class2	Number of received frames classified to QoS class 2.
RX	29	Class3	Number of received frames classified to QoS class 3.

6.8.8 MII Management Bus Block Registers (Block 3)

The following section lists the registers for the MII Management bus block.

Table 132. MII-M Status—MIIMSTAT (Address 0x00)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
3	BUSY	R/O	The bus is currently active.	0x0
1	READING	R/O	A read operation is in progress.	0x0
0	WRITING	R/O	A write operation is in progress.	0x0
This register provides the status of the management bus.				

Table 133. MII-M Command—MIIMCMD (Address 0x01)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
27	SCAN	R/W	Enable SCAN mode.	0x0
26	OPERATION	R/W	Set MII-M operation to read (1) or write (0).	0x0
25:21	PHY_ADDR	R/W	Address of PHY to operate on.	0x00
20:16	PHY_REG	R/W	Register number for operation.	0x00
15:0	WRITE_DATA	R/W	Data to write in write operations.	0x0000
An operation commences when this register is written.				

Table 134. MII-M Return Data—MIIMDATA (Address 0x02)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
16	FAILURE	R/O	Operation failed, no PHY read reply.	0x0
15:0	READ_DATA	R/O	Read data.	0x0000

Table 135. MII-M Prescaler—MIIMPRES (Address 0x03)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
6	NO_PREAMBLE	R/W	When set, no preamble is prepended to the bitstream on the MDIO line. This speeds up PHY register accesses by approximately 50% but may not be compliant with all PHYs.	0x0
5:0	PRESCALE_VALUE	R/W	The divisor for the MIIM clock. A 78.7-MHz clock is divided by (this value + 1). Default clock with default value at approximately 2.4 MHz. The register must not be configured to anything less than 3. For more information about specifications, see "AC Specifications for MII Management," page 233.	0x20

Table 136. MII-M Scan Setup—MIIMSCAN (Address 0x04)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
25:21	PHY_ADDR_HIGH	R/W	This is the upper limit for the PHY addresses to be scanned.	0x00
20:16	PHY_ADDR_LOW	R/W	This is the low limit for the PHY addresses to be scanned.	0x00
15:0	PHY_REG_MASK	R/W	The MASK with target bits in the PHY replies.	0x0000
When the SCAN bit is set in the MIIMCMD register, the operation set up is repeated indefinitely until the bit is reset by a register write. The PHY address loops between the lower and upper limits of the address. For a read operation, the scan results register bit (PHY_ADDR) receives a value of 1 if (PHY_REPLY and PHY_MASK)=PHY_MASK; otherwise. it receives the value of 0. Using this mechanism, it is possible to have an updated link state vector for all 32 PHYs attached to the MII-M bus.				

Table 137. MII-M Scan Results—MIIMSRES (Address 0x05)
Block 3 Subblock 0-1

Bit	Name	Mode	Description	Default
31:0	MIIMSRES	R/O	The scan results as explained above.	0x00000000

6.8.9 Memory Initialization Block Registers (Block 3)

The following section lists the registers for the memory initialization block.

Table 138. Initialize—MEMINIT (Address 0x00)
Block 3 Subblock 2

Bit	Name	Mode	Description	Default
24:8	MEMORY_OPERATION	R/W	For proper initialization of RAM, this field *must* be written 0x10104.	0x0000
7:0	MEMORY_ID	R/W	The identifier for the RAM, which is to be initialized. Range is 0 through 15.	0x00

6.8.10 Frame Arbiter Block Registers (Block 5)

The following section lists the registers for the frame arbiter block.

Table 139. Arbiter Empty—ARBEMPTY (Address 0x0C)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
7:0	ARBEMPTY	R/O	Status per source port. No frame is pending from this source.	0xFF
This register is to be used when resetting a port to stop interaction with other ports before shutting the port down. A correct port reset sequence is: **1.** Disable Rx on the port through MAC::MAC_CFG. **2.** Discard all frames in Arbiter for the port through ARBITER::ARBDISC. **3.** Wait for ARBITER::ARBEMPTY bit for the port to be set. **4.** Set all reset bits in MAC::MAC_CFG.				

Table 140. Arbiter Discard—ARBDISC (Address 0x0E)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
7:0	ARBDISC	R/W	Configuration bit per port. All frames from a source are discarded if the source corresponding bit is set in this register.	0x00

Table 141. Backward for Source—SBACKWDROP (Address 0x12)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
7:0	MASK	R/W	Bit<n> set allows backward dropping of frames from port <n>.	0xFF

Table 142. Backward for Destination—DBACKWDROP (Address 0x13)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
7:0	MASK	R/W	Bit<n> set allows backward dropping of frames destined for port <n>.	0xFF

Table 143. Burst Probability—ARBBURSTPROB (Address 0x15)
Block 5 Subblock 0

Bit	Name	Mode	Description	Default
3:0	PROBABILITY	R/W	Selects the probability of the same source port being allowed to forward to a destination port twice, even though multiple ports have pending frames in their ingress queues. The probability is <this value> / 16. Set this to above zero to guarantee fairness in all situations.	0x0

6.8.11 CPU_CAPT Block Registers (Block 4)

This block only holds one register, which is replicated 256 times. In auto-window mode, only the first address should be read. In non-auto-window mode, all addresses are valid.

Table 144. Frame Data—FRAME_DATA (Addresses 0x00-0xFF)
Block 4 Subblock 0-3

Bit	Name	Mode	Description	Default
31:0	FRAME_DATA	R/W	Frame data.	0x00000000

6.8.12 CPU_CAPT_CTRL Block Registers (Block 4)

The registers described here are used for accessing capture queue 0 and 1. The registers in subblock 4 access capture queue 0, and the registers in subblock 6 access capture queue 1.

Table 145. Read Pointer—CAPREADP (Address 0x00)
Block 4 Subblock 4, 6

Bit	Name	Mode	Description	Default
10:0	CAPREADP	R/W	The physical address of the first frame for reading. The RAM cells are eight bytes wide.	0x000
Write anything to this register, and the read pointer is advanced to the next frame for readout.				

Table 146. Write Pointer—CAPWRP (Address 0x03)
Block 4 Subblock 4, 6

Bit	Name	Mode	Description	Default
17	FRAME_READY	R/O	A frame is ready for readout. Note that buffer address 0 is always pointing to the next frame available.	0x0
16	FRAME_DROPPED	R/W	A frame for the CPU buffer is dropped due to lack of buffer space.	0x0
10:0	CAPWRP	R/O	The physical address of the start of the next incoming frame.	0x000
The FRAME_DROPPED status bit is cleared by writing anything to this register.				

6.8.13 CPU_CAPT_RST Block Registers (Block 4)

The following section lists the registers for the CPU_CAPT_RST block.

Table 147. Full Reset—CAPRST (Address 0xFF)
Block 4 Subblock 7

Bit	Name	Mode	Description	Default
31:0	CAPRST	W/O	Writing anything to this register resets the CPU receive block.	0x00000000
Note that this register is only present in subblock 7.				

6.8.14 Frame Analyzer Block Registers (Block 2)

The following section lists the registers for the frame analyzer block.

Table 148. Flooding Storm Control—STORMLIMIT (Address 0x02)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31	ENABLE_BC	R/W	Only limit the amount of flooded broadcast frames when this field is set.	0x0
30	ENABLE_MC	R/W	Only limit the amount of flooded multicast frames when this field is set.	0x0
29	ENABLE_UC	R/W	Only limit the amount of flooded unicast frames when this field is set.	0x0
27:24	MAXBURST	R/W	Maximum number of frames in a storm burst is $2^{<\text{this field}>}$.	0x0
23:16	MAXRATE_BC	R/W	Rate of broadcasts allowed. Unit is 991 frames per second.	0x00
15:8	MAXRATE_MC	R/W	Rate of multicasts allowed. Unit is 991 frames per second.	0x00
7:0	MAXRATE_UC	R/W	Rate of unicasts allowed. Unit is 991 frames per second.	0x00

Table 149. Advanced Learning Setup—ADVLEARN (Address 0x03)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31	AUTO_MODE	R/W	Unicast source addresses are automatically inserted into the MAC table.	0x1
30	DROP_MODE	R/W	Frames subject to learning or station port move are not forwarded based on the destination address.	0x0
29	VLAN_CHK	R/W	If a frame is discarded because of the VLAN_SRC_CHK flag in the VLAN table (see VLANACCESS register) or the VLANMASK, the source address is not learned.	0x0

Table 149. Advanced Learning Setup—ADVLEARN (Address 0x03) *(continued)*
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
26	CPU_LEARN	R/W	Learn frames are forwarded to the CPU capture module.	0x0
7:0	LEARN_MIRROR	R/W	Learn frames are also forwarded to ports marked in this mask.	0x00

Table 150. IP Multicast Flood Mask—IFLODMSK (Address 0x04)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	IFLODMSK	R/W	Port mask with allowed ports for unknown IP multicast flooding. This is overruled if AGENCTRL::FLOOD_FWD_KILL is set.	0x00

Table 151. VLAN Source Port Mask—VLANMASK (Address 0x05)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	VLANMASK	R/W	Mask for requiring VLAN Source Check on ingress port. If bit<port> is set, the <port> must be marked in the ingress frame's VLAN port mask; otherwise, the frame is dropped.	0x00

Table 152. MAC Address High—MACHDATA (Address 0x06)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27:16	VID	R/W	VID to be used in MAC CPU write operations. Additionally, VID is returned in read operations.	0x000
15:0	MAC_ADDR_HIGH	R/W	Upper 16 MAC address bits for CPU write operations. Additionally, MAC_ADDR_HIGH is returned in read operations.	0x0000

Table 153. MAC Address Low—MACLDATA (Address 0x07)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31:0	MACLDATA	R/W	Lower 32 MAC address bits for CPU operations.	0x00000000

Table 154. Station Move Logger—ANMOVED (Address 0x08)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	ANMOVED	R/W	Sticky bit set when a station is learned on a port while already learned on another port.	0x00
The register is cleared by writing the bits to be cleared. This mask can be used to detect topology problems in the network, where stations are learned on multiple ports repeatedly. If some bits in this register get asserted repeatedly, the ports can be shut down or management warnings can be issued.				

Table 155. Aging Filter—ANAGEFIL (Address 0x09)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31	PID_EN	R/W	If set, only entries with a destination matching PID_VAL are aged.	0x0
18:16	PID_VAL	R/W	Destination port number. Used to identify which entries in a MAC table are to be aged. Only used if PID_EN is set.	0x0
15	VID_EN	R/W	If set, only entries with a VLAN identifier matching VID_VAL are aged.	0x0
11:0	VID_VAL	R/W	VLAN identifier. Used to identify which entries in the MAC table are to be aged. Only used if VID_EN is set.	0x000
This register sets up which entries should be touched by an aging operation. In this way, it is possible to have different aging periods in each VLAN and to have quick removal of entries on specific ports.				

Table 156. Event Sticky Bits—ANEVENTS (Address 0x0A)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
22	STORM_DROP	R/W	A frame was dropped, because it exceeded the flooding storm limitations configured in STORMLIMIT.	0x0
21	LEARN_DROP	R/W	A frame was dropped, because it was subject to learning, and the DropMode flag was set in ADVLEARN.	0x0
20	AGED_ENTRY	R/W	An entry was removed at CPU learn or CPU requested an aging process.	0x0
19	CPU_LEARN_FAILED	R/W	A learn failed due to hash table depletion.	0x0
18	AUTO_LEARN_FAILED	R/W	A learn of incoming source MAC address failed due to hash table depletion.	0x0
17	LEARN_REMOVE	R/W	An entry was removed when learning a new source MAC address.	0x0
16	AUTO_LEARNED	R/W	An entry was learned from an incoming frame.	0x0
15	AUTO_MOVED	R/W	A station was moved to another port.	0x0
14	DROPPED	R/W	A packet was not transmitted to any ports.	0x0

Table 156. Event Sticky Bits—ANEVENTS (Address 0x0A) *(continued)*
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
13	CLASSIFIED_DROP	R/W	A packet was not forwarded due to classification (like BPDUs).	0x0
12	CLASSIFIED_COPY	R/W	A packet was copied to the CPU due to classification.	0x0
11	VLAN_DISCARD	R/W	A packet was discarded due to lack of VLAN membership on source port.	0x0
10	FWD_DISCARD	R/W	A packet was discarded due to missing forwarding state on source port.	0x0
9	MULTICAST_FLOOD	R/W	A packet was flooded with multicast flooding mask.	0x0
8	UNICAST_FLOOD	R/W	A packet was flooded with unicast flooding mask.	0x0
7	DEST_KNOWN	R/W	A packet was forwarded with known destination MAC address.	0x0
6	BUCKET3_MATCH	R/W	A destination was found in hash table bucket 3.	0x0
5	BUCKET2_MATCH	R/W	A destination was found in hash table bucket 2.	0x0
4	BUCKET1_MATCH	R/W	A destination was found in hash table bucket 1.	0x0
3	BUCKET0_MATCH	R/W	A destination was found in hash table bucket 0.	0x0
2	CPU_OPERATION	R/W	A CPU initiated operation was processed.	0x1
1	DMAC_LOOKUP	R/W	A destination address was looked up in the MAC table.	0x0
0	SMAC_LOOKUP	R/W	A source address was looked up in the MAC table.	0x0
This register contains various debug event logs. A sticky bit is cleared by writing to it.				

Table 157. Event Sticky Mask—ANCNTMSK (Address 0x0B)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
22:0	STICKY_MASK	R/W	This mask determines which events are counted by the ANCNTVAL register.	0x000000
For proper operation, only one bit should be set in the mask. Otherwise, if two events occur simultaneously, they may be mistaken for only one event and counted as only one event in the ANCNTVAL register. For more information, see the flag list in the ANEVENTS register.				

Table 158. Event Sticky Counter—ANCNTVAL (Address 0x0C)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27:0	ANCNTVAL	R/W	This counter counts the number of events seen as specified in the Event Sticky Mask.	0x0000000

Table 159. Learn Mask—LEARNMASK (Address 0x0D)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	LEARNMASK	R/W	If bit<port> is set in this mask, incoming frames are subject to auto learning on that port.	0xFF

Table 160. Unicast Flood Mask—UFLODMSK (Address 0x0E)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	UFLODMSK	R/W	Port mask with allowed ports for unknown unicast flooding.	0xFF

Table 161. Multicast Flood Mask—MFLODMSK (Address 0x0F)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	MFLODMSK	R/W	Port mask with allowed ports for unknown multicast flooding and for broadcast flooding.	0xFF

Table 162. Receive Mask—RECVMASK (Address 0x10)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	RECVMASK	R/W	If a port is not marked in this mask, incoming frames are discarded.	0x00

Table 163. Aggregation Mode—AGGRCTRL (Address 0x20)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
2:0	AGGRCTRL	R/W	Mode of aggregation: 000: SMAC xor DMAC xor IP-info. 001: SMAC. 010: DMAC. 011: SMAC xor DMAC. 100: Pseudo randomized. 101: IP-info.	0x1

Table 164. Aggregation Masks—AGGRMSKS (Addresses 0x30-0x3F)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	MASK	R/W	Mask used to select only one port within each aggregation group.	0xFF
These 16 masks select a single port in each aggregated port group. If no aggregation is configured, these masks are all-ones.				

Table 165. Destination Port Masks—DSTMASKS (Addresses 0x40-0x7F)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
7:0	DST_MASK	R/W	Mask used to translate a logical port number from a destination lookup into a set of ports.	See note at end of table.
By default, port masks 0-4, 6 have the bit corresponding to their number set only. The remaining are cleared to 0 for multicasts. In normal situations, it does not make sense to change port masks 0-4, 6 from the default, except in aggregation setups. Otherwise, frames for a station would be transmitted on another port than the port on which it was auto learned.				

Table 166. Source Port Masks—SRCMASKS (Addresses 0x80-0x87)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27	CPU_COPY	R/W	All frames from this port are copied to the CPU capture buffer.	0x0
26	MIRROR	R/W	All frames from this port are mirrored to the port set in the analyzer configuration register.	0x0
7:0	PORTS	R/W	Mask used to disallow frames from being forwarded from a specific source port.	See note at end of table.
These masks are used to prevent frames from being looped back to the ports on which they were received and must be updated according to the aggregation configuration. A frame that is received on port n, uses register 0x80 + n as a mask to filter out transmit ports to avoid loop back or to facilitate port grouping (port-based VLANs). The default values are that all bits are set except for the index number. For example, srcmask 3 has a default value of 0b00010111, or 0x17.				

Table 167. Capture Enabled—CAPENAB (Address 0xA0)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
20	IPMC	R/W	IP multicast control capture when this field is set.	0x0
19	ARPBC	R/W	ARP broadcast capture is enabled when this field is set.	0x0
18	IGMP	R/W	IGMP snooping is enabled when this field is set.	0x0
17	ALLBRIDGE	R/W	All LANs Bridge Management Group Frames (DMAC=01-80-C2-00-00-10) capturing is enabled when this field is set.	0x0

Table 167. Capture Enabled—CAPENAB (Address 0xA0) *(continued)*
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
16	BPDU	R/W	Bridge control frames (DMAC=01-80-C2-00-00-0x) capturing is enabled when this field is set.	0x0
15:0	GARP	R/W	GARP frame is (DMAC=01-80-C2-00-00-2x) capturing is enabled when this field is set. There is one configuration bit per address.	0x0000

Table 168. MAC Table Command—MACACCESS (Address 0xB0)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
14	CPU_COPY	R/W	Frames with this MAC are copied to the CPU capture buffer.	0x0
13	FWD_KILL	R/W	Frames with this MAC are dropped.	0x0
12	IGNORE_VLAN	R/W	The VLAN mask is ignored for this destination.	0x0
11	AGED_FLAG	R/W	This flag is set on every aging run. Entry is removed if set already. The flag is cleared when the entry is targetted for a source address lookup. Locked entries are not touched by the aging process. If the AGED_FLAG is set for locked entries, the entry is interpreted as an IPMC entry.	0x0
10	VALID	R/W	Entry is valid.	0x0
9	LOCKED	R/W	Entry is locked and is not removed by aging or auto-learn pushout. Port move events are only registered in ANMOVE if a MAC address is learned with the lock flag cleared.	0x0
8:3	DEST_IDX	R/W	Index for the destination mask table. For unicasts, this is a number from 0-4, 6.	0x00
2:0	MAC_TABLE_CMD	R/W	MAC table command.	0x0

The MACACCESS register is used for updating or reading the MAC table from the CPU. The command selects between different operations and uses the following encoding:

- 000: Idle—The previous operation is complete.
- 001: Learn—The MAC data is learned into the table.
- 010: Forget—The MAC data is removed from the table.
- 011: Age table—The aging procedure is performed on the table.
- 100: Flush table—All non-locked entries are removed from the table.
- 101: Clear table—Table is completely cleared.
- 110: Read entry—The entry pointed to by the MAC Table Index register is read.
- 111: Write entry—The entry pointed to by the MAC Table Index register is written.

A table age/clear/flush command runs for approximately 50 µs. The other commands execute immediately.

Table 169. IPMC Access—IPMCACCESS (Address 0xB1)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
31	IPMC_EN	R/W	Enable IPMC programming mode. This field must be set for programming IP multicast entries into the MAC table.	0x0
7:0	IPMCPORTS	R/W	Destination mask for IPMC group.	0x00

Table 170. MAC Table Index—MACTINDX (Address 0xC0)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
13	SHADOW	R/W	Enable MAC table shadow register. With this register set when reading from bucket 0, the remaining three buckets are latched into a register for future access.	0x0
12:11	BUCKET	R/W	The bucket selects one of the four entries per table line.	0x0
10:0	INDEX	R/W	The index selects one of the 2048 MAC table lines.	0x000
Used in MAC table read and write operations where this register selects the entry to read or write.				

Table 171. VLAN Table Command—VLANACCESS (Address 0xD0)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
30	VLAN_LEARN_DISABLED	R/W	Disable learning for this VLAN,	0x0
29	VLAN_MIRROR	R/W	Set if all frames in this VLAN are to be mirrored onto the port specified in the analyzer configuration register.	0x0
28	VLAN_SRC_CHK	R/W	Set if the source port for frames in this VLAN must be marked in the VLAN port mask.	0x0
9:2	VLAN_PORT_MASK	R/W	Frames in this VLAN may only be sent to ports in this mask.	0xFF
1:0	VLAN_TBL_CMD	R/W	VLAN table command.	0x0

The VLANACCESS register is used for updating and reading the VLAN table from the CPU. The command selects between different operations and uses the following encoding:

- 00: Idle—The previous operation is complete.
- 01: Read entry—The entry set in VLAN index is read out into this register.
- 10: Write entry—The entry set in VLAN index is written.
- 11: Clear Table—The VLAN table is initialized to default values.

The VLAN table command field must read Idle before a new command can be issued. The execution times are the same as for the MACACCESS register. For more information, see "MAC Table Command—MACACCESS (Address 0xB0)," page 186.

Table 172. VLAN Table Index—VLANTIDX (Address 0xE0)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
11:0	INDEX	R/W	The index selects one of the 4096 VLAN table lines.	0x000
Used in VLAN table read and write operations where this register selects the entry to read or write.				

Table 173. Analyzer Configuration Register—AGENCTRL (Address 0xF0)
Block 2 Subblock 0

Bit	Name	Mode	Description	Default
27:16	FID_MASK	R/W	Mask bits set in this field from the VID when looking up stations in the MAC table.	0x000
14	IGNORE_DMAC_FLAGS	R/W	Do not react on flags found in the DMAC record.	0x0
13	IGNORE_SMAC_FLAGS	R/W	Do not react on flags found in the SMAC record.	0x0
11	FLOOD_CPU_COPY	R/W	Flooded frames are copied to the CPU.	0x0
10	FLOOD_FWD_KILL	R/W	Flooded frames are not sent to any ports.	0x0
9	FLOOD_IGNORE_VLAN	R/W	Flooded frames are not sensitive to the VLAN masks.	0x0
8	MIRROR_CPU	R/W	Frames destined for the CPU capture buffer are also forwarded to the configured mirror port.	0x0
7	LEARN_CPU_COPY	R/W	Auto-learned stations have the CPU_COPY flag set in their entry in the MAC table.	0x0
6	LEARN_FWD_KILL	R/W	Auto-learned stations have the FwdKill flag set in their entry in the MAC table.	0x0
5	LEARN_IGNORE_VLAN	R/W	Auto-learned stations have the Ignore VLAN flag set in their entry in the MAC table.	0x0
2:0	MIRROR_PORT	R/W	Frames mirrored are sent to this port.	0x0

6.8.15 Standard Set PHY Registers

The following section lists the registers for the Standard Set PHY.

Table 174. Control—PHY_CTRL (Address 0x00)
PHY Register

Bit	Name	Mode	Description	Default
15	SOFTWARE_RESET_ENA	R/W	Initiate software reset. This field is cleared as part of this operation. After enabling this field, you must wait at least 4 µs before PHY registers can be accessed again.	0x0
14	LOOPBACK_ENA	R/W	Enable loopback mode. The loopback mechanism works at the current speed. If the link is down (see PHY_STAT::LINK_STATUS), SPEED_SEL_LSB_CFG and SPEED_SEL_MSB_CFG determine the operating speed of the loopback.	0x0

Table 174. Control—PHY_CTRL (Address 0x00) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
13	SPEED_SEL_LSB_CFG	R/W	Least significant bit of the speed selection, along with SPEED_SEL_MSB_CFG, this field determines the speed when auto-negotiation is disabled (see AUTONEG_ENA). 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	0x0
12	AUTONEG_ENA	R/W	Enable auto-negotiation. When cleared, the speed and duplex-mode is determined by SPEED_SEL_LSB_CFG, SPEED_SEL_MSB_CFG, and DUPLEX_MODE_CFG.	0x1
11	POWER_DOWN_ENA	R/W	Enable power-down mode. This disables PHY operation until this bit is cleared or the PHY is reset.	0x0
10	ISOLATE_ENA	R/W	Isolate the PHY from the integrated MAC.	0x0
9	AUTONEG_RESTART_ENA	R/W	Restart an auto-negotiation cycle; the PHY clears this field when auto-negotiation is restarted.	0x0
8	DUPLEX_MODE_CFG	R/W	Configure duplex mode when auto-negotiation is disabled (see AUTONEG_ENA). 0: Half-duplex. 1: Full-duplex.	0x0
7	COLLISION_TEST_ENA	R/W	Enable collision indication test-mode, when enabled the PHY indicate collision when the MAC transmits data to the PHY.	0x0
6	SPEED_SEL_MSB_CFG	R/W	See SPEED_SEL_LSB_CFG.	0x1
5:0	RESERVED	R/W	Must be default value.	0x00

Table 175. Status—PHY_STAT (Address 0x01)
PHY Register

Bit	Name	Mode	Description	Default
15	MODE_100BT4	R/O	SparX-G5e PHY is not 100BASE-T4 capable.	0x0
14	MODE_100BX_FDX	R/O	SparX-G5e PHY is 100BASE-X FDX capable.	0x1
13	MODE_100BX_HDX	R/O	SparX-G5e PHY is 100BASE-X HDX capable.	0x1
12	MODE_10BT_FDX	R/O	SparX-G5e PHY is 10BASE-T FDX capable.	0x1
11	MODE_10BT_HDX	R/O	SparX-G5e PHY is 10BASE-T HDX capable.	0x1
10	MODE_100BT2_FDX	R/O	SparX-G5e PHY is not 100BASE-T2 FDX capable.	0x0
9	MODE_100BT2_HDX	R/O	SparX-G5e PHY is not 100BASE-T2 HDX capable.	0x0
8	EXT_STATUS	R/O	Extended status information are available; see register PHY_STAT_EXT.	0x1
7	RESERVED	R/O	Reserved.	0x0
6	PREAMBLE_SUPPRESS	R/O	SparX-G5e PHY accepts management frames with preamble suppressed.	0x1

Table 175. Status—PHY_STAT (Address 0x01) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
5	AUTONEG_COMPLETE	R/O	This field is set when auto-negotiation is completed and cleared during active auto-negotiation cycles.	0x0
4	REMOTE_FAULT	R/O	This field is set when the PHY detects a remote fault condition and cleared on register read.	0x0
3	AUTONEG_ABILITY	R/O	SparX-G5e PHY is capable of auto-negotiation.	0x1
2	LINK_STAT	R/O	This field is cleared when the link is down. It is set when the link is up and a previous link-down indication was read from the register.	0x0
1	JABBER_DETECT	R/O	This field is set when the PHY detects a Jabber condition and cleared on register read.	0x0
0	EXT_CAPABILITY	R/O	SparX-G5e PHY provides an extended set of capabilities.	0x1

Table 176. Identifier Number 1—PHY_IDF1 (Address 0x02)
PHY Register

Bit	Name	Mode	Description	Default
15:0	OUI_MS	R/O	Vitesse's organizationally unique identifier bits 3 through 18.	0x0007

Table 177. Identifier Number 2—PHY_IDF2 (Address 0x03)
PHY Register

Bit	Name	Mode	Description	Default
15:10	OUI_LS	R/O	Vitesse's organizationally unique identifier bits 19 through 24.	0x01
9:4	MODEL_NUMBER	R/O	SparX-G5e model number.	0x15
3:0	REVISION_NUMBER	R/O	SparX-G5e revision number.	0x2

Table 178. Auto-Negotiation Advertisement—PHY_AUTONEG_ADVERTISMENT (Address 0x04)
PHY Register

Bit	Name	Mode	Description	Default
15	NEXT_PAGE_ENA	R/W	Advertises desire to engage in next-page exchange. When this field is set, next-page control is returned to the user for additional next-pages following the 1000BASE-T next-page exchange.	0x0
14	RESERVED	R/W	Must be default value.	0x0
13	REMOTE_FAULT_CFG	R/W	Transmit remote fault.	0x0
12	RESERVED	R/W	Must be default value.	0x0
11	ASSYM_PAUSE_CFG	R/W	Advertise asymmetric pause capability.	0x0

Table 178. Auto-Negotiation Advertisement—PHY_AUTONEG_ADVERTISMENT (Address 0x04) *(continued)*

Bit	Name	Mode	Description	Default
10	SYM_PAUSE_CFG	R/W	Advertise symmetric pause capability.	0x0
9	ADV_100BT4_CFG	R/W	Advertise 100BASE-T4 capability.	0x0
8	ADV_100BX_FDX_CFG	R/W	Advertise 100BASE-X FDX capability.	0x1
7	ADV_100BX_HDX_CFG	R/W	Advertise 100BASE-X HDX capability.	0x1
6	ADV_10BT_FDX_CFG	R/W	Advertise 10BASE-T FDX capability.	0x1
5	ADV_10BT_FDX_CFG	R/W	Advertise 10BASE-T HDX capability.	0x1
4:0	SELECTOR_FIELD_CFG	R/W	Select types of message send by auto-negotiation.	0x01

Table 179. Auto-Negotiation LP Base Page Ability—PHY_AUTONEG_LP_ABILITY (Address 0x05) PHY Register

Bit	Name	Mode	Description	Default
15	LP_NEXT_PAGE	R/O	Link partner advertises desire to engage in next-page exchange.	0x0
14	LP_ACKNOWLEDGE	R/O	Link partner advertises that link code word was successfully received.	0x0
13	LP_REMOTE_FAULT	R/O	Link partner advertises remote fault.	0x0
12	RESERVED	R/O	Reserved.	0x0
11	LP_ASSYM_PAUSE	R/O	Link partner advertises asymmetric pause capability.	0x0
10	LP_SYM_PAUSE	R/O	Link partner advertises symmetric pause capability.	0x0
9	LP_100BT4	R/O	Link partner advertises 100BASE-T4 capability.	0x0
8	LP_100BX_FDX	R/O	Link partner advertises 100BASE-X FDX capability.	0x0
7	LP_100BX_HDX	R/O	Link partner advertises 100BASE-X HDX capability.	0x0
6	LP_10BT_FDX	R/O	Link partner advertises 10BASE-T FDX capability.	0x0
5	LP_10BT_FDX	R/O	Link partner advertises 10BASE-T HDX capability.	0x0
4:0	LP_SELECTOR_FIELD	R/O	Link partner advertises select type of message send by auto-negotiation.	0x00

Table 180. Auto-Negotiation Expansion—PHY_AUTONEG_EXP (Address 0x06) PHY Register

Bit	Name	Mode	Description	Default
15:5	RESERVED	R/O	Reserved.	0x000
4	PARALLEL_DET_FAULT	R/O	This field is set when the PHY detects a Receive Link Integrity Test failure condition and cleared on register read.	0x0
3	LP_NEXT_PAGE_ABLE	R/O	Set if link partner is next-page capable.	0x0
2	NEXT_PAGE_ABLE	R/O	SparX-G5e PHY is next-page capable.	0x1

**Table 180. Auto-Negotiation Expansion—PHY_AUTONEG_EXP (Address 0x06) *(continued)*
PHY Register**

Bit	Name	Mode	Description	Default
1	NEXT_PAGE_RECEIVED	R/O	This field is set when the PHY receives a valid next page and cleared on register read.	0x0
0	LP_AUTONEG_ABLE	R/O	Set if link partner is auto-negotiation capable.	0x0

**Table 181. Auto-Negotiation Next Page Transmit—PHY_AUTONEG_NEXTPAGE_TX
(Address 0x07) PHY Register**

Bit	Name	Mode	Description	Default
15	NEXT_PAGE_CFG	R/W	Set to indicate that more pages follow; clear if current page is the last.	0x0
14	RESERVED	R/W	Must be default value.	0x0
13	MESSAGE_PAGE_CFG	R/W	Set to indicate that this is a message page; clear if the current page consists of unformatted code.	0x1
12	ACKNOWLEDGE2_CFG	R/W	Set to indicate ability to comply with the request of the last received page.	0x0
11	TOGGLE	R/O	Alternates between 0 and 1 for each transmitted page.	0x0
10:0	MESSAGE_FIELD_CFG	R/W	Contains page information – either message or unformatted code. MESSAGE_PAGE_CFG must indicate if this page contains either a message or unformatted code.	0x001

**Table 182. Auto-Negotiation LP Next Page Receive—PHY_AUTONEG_LP_NEXTPAGE_RX
(Address 0x08) PHY Register**

Bit	Name	Mode	Description	Default
15	LP_NEXT_PAGE	R/O	Set by link partner to indicate that more pages follow. When cleared, this is the last of the next pages.	0x0
14	LP_ACKNOWLEDGE	R/O	Set by link partner to acknowledge the reception of last message.	0x0
13	LP_MESSAGE_PAGE	R/O	Set by link partner if this page contains a message. When cleared, this page contains unformatted code.	0x0
12	LP_ACKNOWLEDGE2	R/O	Set by link partner to indicate that it is able to act on transmitted information.	0x0
11	LP_TOGGLE	R/O	Alternates between 0 and 1 for each received page. Used to check for errors.	0x0
10:0	LP_MESSAGE_FIELD	R/O	Contains page information. MESSAGE_PAGE indicates whether this page contains a message or unformatted code.	0x000

Table 183. 1000BASE-T Control—PHY_CTRL_1000BT (Address 0x09) PHY Register

Bit	Name	Mode	Description	Default
15:13	TX_TEST_MODE_CFG	R/W	Configure 1000BASE-T test modes; this field is only valid in 1000BASE-T mode. Other encodings are reserved and must not be selected. 000: Normal operation. 001: Transmit waveform test. 010: Transmit jitter test in master mode. 011: Transmit jitter test in slave mode. 100: Transmit distortion test.	0x0
12	MS_MANUAL_CFG_ENA	R/W	Enable manual configuration of master/slave value.	0x0
11	MS_MANUAL_CFG	R/W	Configure if the PHY should configure itself as either master or slave during master/slave negotiations. This field is only valid when MANUAL_CFG_ENA is set. 0: Configure as slave. 1: Configure as master.	0x0
10	PORT_TYPE_CFG	R/W	Set to indicate multi-port device, clear to indicate single-port device.	0x1
9	ADV_1000BT_FDX_CFG	R/W	Set to advertise 1000BASE-T FDX capability.	0x1
8	ADV_1000BT_HDX_CFG	R/W	Set to advertise 1000BASE-T HDX capability.	0x1
7:0	RESERVED	R/W	Must be default value.	0x00

Table 184. 1000BASE-T Status—PHY_STAT_1000BT (Address 0x0A) PHY Register

Bit	Name	Mode	Description	Default
15	MS_CFG_FAULT	R/O	This field is set when the PHY detects a master/slave configuration fault condition and cleared on register read.	0x0
14	MS_CFG_RESOLUTION	R/O	This field indicates the result of a master/slave negotiation. 0: Local PHY is resolved to slave. 1: Local PHY is resolved to master.	0x1
13	LOCAL_RECEIVER_STAT	R/O	The status of the local receiver (loc_rcvr_status as defined in IEEE Std. 802.3). 0: Local receiver status is NOT_OK. 1: Local receiver status is OK.	0x0
12	REMOTE_RECEIVER_STAT	R/O	The status of the remote receiver (rem_rcvr_status as defined in IEEE Std. 802.3). 0: Remote receiver status is NOT_OK. 1: Remote receiver status is OK.	0x0
11	LP_1000BT_FDX	R/O	Set if link partner advertises 1000BASE-T FDX capability.	0x0
10	LP_1000BT_HDX	R/O	Set if link partner advertises 1000BASE-T HDX capability.	0x0
9:8	RESERVED	R/O	Reserved.	0x0

Table 184. 1000BASE-T Status—PHY_STAT_1000BT (Address 0x0A) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
7:0	IDLE_ERR_CNT	R/O	Counts each occurrence of rxerror_status=Error (rxerror_status as defined in IEEE Std. 802.3). This field is cleared on read and saturates at all-ones.	0x00

Table 185. Extended Status—PHY_STAT_EXT (Address 0x0F)
PHY Register

Bit	Name	Mode	Description	Default
15	MODE_1000BX_FDX	R/O	SparX-G5e PHY is not 1000BASE-X FDX capable.	0x0
14	MODE_1000BX_HDX	R/O	SparX-G5e PHY is not 1000BASE-X HDX capable.	0x0
13	MODE_1000BT_FDX	R/O	SparX-G5e PHY is 1000BASE-T FDX capable.	0x1
12	MODE_1000BT_HDX	R/O	SparX-G5e PHY is 1000BASE-T HDX capable.	0x1
11:0	RESERVED	R/O	Reserved.	0x000

Table 186. 100BASE-TX Status—PHY_STAT_100BTX (Address 0x10)
PHY Register

Bit	Name	Mode	Description	Default
15	DESCRAM_LOCKED	R/O	This field is set when the 100BASE-TX descrambler is in lock and is cleared when it is out of lock.	0x0
14	DESCRAM_ERR	R/O	This field is set when the phy detects a descrambler error condition and is cleared on register read.	0x0
13	LINK_DISCONNECT	R/O	This field is set when the PHY detects a 100BASE-TX link disconnect condition and is cleared on register read.	0x0
12	LINK_STAT	R/O	This field is set when the 100BASE-TX link status is active and is cleared when inactive.	0x0
11	RECEIVE_ERR	R/O	This field is set when the PHY detects a receive error condition and is cleared on register read.	0x0
10	TRANSMIT_ERR	R/O	This field is set when the PHY detects a transmit error condition and is cleared on register read.	0x0
9	SSD_ERR	R/O	This field is set when the PHY detects a start-of-stream delimiter error condition and is cleared on register read.	0x0
8	ESD_ERR	R/O	This field is set when the PHY detects a end-of-stream delimiter error condition and is cleared on register read.	0x0
7:0	RESERVED	R/O	Reserved.	0x00
These fields are only valid in 100BASE_T mode.				

Table 187. Extended 1000BASE-T Status—PHY_STAT_1000BT_EXT (Address 0x11) PHY Register

Bit	Name	Mode	Description	Default
15	DESCRAM_LOCKED	R/O	This field is set when the 1000BASE-T descrambler is in lock and is cleared when it is out of lock.	0x0
14	DESCRAM_ERR	R/O	This field is set when the PHY detects a Descrambler Error condition and is cleared on register read.	0x0
13	LINK_DISCONNECT	R/O	This field is set when the PHY detects a 1000BASE-T link disconnect condition and is cleared on register read.	0x0
12	LINK_STAT	R/O	This field is set when the 1000BASE-T link status is active and is cleared when inactive.	0x0
11	RECEIVE_ERR	R/O	This field is set when the PHY detects a Receive Error condition and is cleared on register read.	0x0
10	TRANSMIT_ERR	R/O	This field is set when the PHY detects a Transmit Error condition and is cleared on register read.	0x0
9	SSD_ERR	R/O	This field is set when the PHY detects a Start-of-Stream Delimiter Error condition and is cleared on register read.	0x0
8	ESD_ERR	R/O	This field is set when the PHY detects a End-of-Stream Delimiter Error condition and is cleared on register read.	0x0
7	CARRIER_EXT_ERR	R/O	This field is set when the PHY detects a 1000BASE-T Carrier Extension Error condition and is cleared on register read.	0x0
6	BCM5400_ERR	R/O	This field is set when the PHY detects a Non-Compliant BCM5400 condition and is cleared on register read. This field is only valid when the 1000BASE-T descambler is in locked state (see DESCRAM_LOCKED).	0x0
5:0	RESERVED	R/O	Reserved.	0x00
These fields are only valid in 1000BASE_T mode.				

Table 188. Bypass Control—PHY_BYPASS_CTRL (Address 0x12) PHY Register

Bit	Name	Mode	Description	Default
15	TX_DIS	R/W	Disable the PHY transmitter. When set, the analog blocks are powered down and zeros are sent to the DAC.	0x0
14:6	RESERVED	R/W	Must be default value.	0x000
5	PAIR_SWAP_DIS	R/W	Disable automatic pair swap correction. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0

Table 188. Bypass Control—PHY_BYPASS_CTRL (Address 0x12) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
4	POL_INV_DIS	R/W	Disable automatic polarity inversion correction. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
3	PARALLEL_DET_DIS	R/W	When cleared, the PHY ignores its advertised abilities when performing parallel detect. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x1
2	RESERVED	R/W	Must be default value.	0x0
1	AUTO_NP_EXCHANGE_DIS	R/W	Disable automatic exchange of 1000BASE-T next pages. If this feature is disabled, you have the responsibility for sending next pages, determining capabilities, and configuration of the PHY after successful exchange of pages. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
0	RESERVED	R/W	Must be default value.	0x0

Table 189. Extended Control and Status—PHY_CTRL_STAT_EXT (Address 0x16)
PHY Register

Bit	Name	Mode	Description	Default
15	LINK_10BT_FORCE_ENA	R/W	When this field is set, the PHY link integrity state machine is bypassed, and the PHY is forced into link pass status. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
14	JABBER_DETECT_DIS	R/W	Disable jabber detect function. When this is disabled, the PHY allows transmission requests to be arbitrarily long without shutting down the transmitter. When cleared, the PHY shuts down the transmitter after the specified time limit as defined by IEEE. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
13	ECHO_10BT_DIS	R/W	When this field is set, the state of the TX_EN pin does not echo onto the CRS pin, which effectively disables CRS from being asserted in half-duplex operation. When cleared, the TX_EN pin is echoed onto the CRS pin. This applies only in 10BASE-T mode. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x1
12	SQE_10BT_DIS	R/W	Disable SQE (Signal Quality Error) pulses on the MAC interface. This applies only in 10BASE-T mode. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x1

Table 189. Extended Control and Status—PHY_CTRL_STAT_EXT (Address 0x16) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
11:10	SQUELCH_10BT_CFG	R/W	Configure squelch control (this only applies in the 10BASE-T mode). This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). 00: The PHY uses the squelch threshold levels prescribed by the IEEE 10BASE-T specification. 01: In this mode, the squelch levels are decreased, which may improve the bit error rate performance on long loops. 10: In this mode, the squelch levels are increased, which may improve the bit error rate in high-noise environments. 11: Reserved.	0x0
9	STICKY_RESET_ENA	R/W	When set, all fields described as sticky retain their value during software reset. When cleared, all fields marked as sticky are reset to their default values during software reset. This does not affect hardware resets. This is a super-sticky field, which means that it always retains its value during software reset.	0x1
8	EOF_ERR	R/O	When set, this field indicates that a defective EOF (End Of Frame) sequence was received since the last time this field was read. This field is self-clearing; that is, it is cleared on read.	0x0
7	LINK_10BT_DISCONNECT	R/O	When set, this field indicates that the carrier integrity monitor broke the 10BASE-T connection since the last read of this bit. This field is self-clearing; that is, it is cleared on read.	0x0
6	LINK_10BT_STAT	R/O	This field is set when a 10BASE-T link is active. Cleared when inactive.	0x0
5:1	RESERVED	R/O	Reserved.	0x00
0	BROADCAST_WRITE_ENA	R/W	Enable any MII write operation (regardless of destination PHY) to be interpreted as a write to this PHY. This only applies to writes; read-operations are still interpreted with correct address. This is particularly useful when similar settings should be propagated to multiple PHYs. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0

Table 190. Extended Control Number 1—PHY_CTRL_EXT1 (Address 0x17) PHY Register

Bit	Name	Mode	Description	Default
15:4	RESERVED	R/W	Must be default value.	0x002
3	FAR_END_LOOPBACK_ENA	R/W	Enable far-end loopback in this PHY. In this mode all incoming traffic on the media interface is retransmitted back to the link partner. In addition, the incoming data also appears on the internal Rx interface to the MAC. Any data send to the PHY from the internal MAC is ignored when this mode is active.	0x0
2:0	RESERVED	R/W	Must be default value.	0x0

Table 191. Extended Control Number 2—PHY_CTRL_EXT2 (Address 0x18) PHY Register

Bit	Name	Mode	Description	Default
15:13	EDGE_RATE_CFG	R/W	Control the transmit DAC slew rate in 100BASE-TX mode only. The difference between each setting is approximately 200 ps to 300 ps, with the +3 setting resulting in the slowest edge rate, and the –4 setting resulting in the fastest edge rate. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). 011: +3 edge rate (slowest). 010: +2 edge rate. 001: +1 edge rate. 000: Nominal edge rate. 111: –1 edge rate. 110: –2 edge rate. 101: –3 edge rate. 100: –4 edge rate (fastest).	0x6
12	PICMG_REDUCED_POWER_ENA	R/W	Enable PICMG reduce power mode: In this mode, portions of the DSP processor are turned off, which reduces the PHY's operating power. The DSP performance characteristics in this mode is configured to support the channel characteristics specified in the PICMG 2.16 and PICMG 3.0 specifications. The application of this mode is in environments that has a high signal to noise ratio on the media. For example, Ethernet over backplane, or where cable length is short (less than 10 m). When this field is cleared, the PHY operates in normal DSP mode. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
11:10	RESERVED	R/W	Must be default value.	0x0

Table 191. Extended Control Number 2—PHY_CTRL_EXT2 (Address 0x18) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
9:7	TX_FIFO_DEPTH_1000BT_CFG	R/W	Controls the symbol buffering for the transmit synchronization FIFO used in 1000BASE-T mode. Other encodings are reserved and must not be selected. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). 100: IEEE mode. This mode supports up to 1518-byte packet size with a minimum inter-packet gap (IPG). 011: Jumbo packet mode. This mode adds latency to the path to support up to 9600-byte packets with a minimum inter-packet gap (IPG). When using this mode, larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.	0x4
6:4	RX_FIFO_DEPTH_1000BT_CFG	R/W	Controls the symbol buffering for the receive synchronization FIFO used in 1000BASE-T mode. Other encodings are reserved and must not be selected. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). 100: IEEE mode. This mode supports up to 1518-byte packet size with a minimum inter-packet gap (IPG). 011: Jumbo packet mode. This mode adds latency to the path to support up to 9600-byte packets with a minimum inter-packet gap (IPG). When using this mode, larger IPG is recommended due to the possible compression of the IPG at the output of the FIFO.	0x4
3:1	DACG_AMPLITUDE_CFG	R/W	Fine control of the amplitude of the 100BASE-T signal waveform. The signal level can be boosted or attenuated from the nominal setting to compensate for variations in characteristics of the magnetics so that the waveform on the media side of the transformer is compliant with the IEEE standard. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). The allowed settings for these bits and the corresponding boost or attenuation amounts are: 011: +6% 010: +4% 001: +2% 000: nominal 111: –2% 110: –4% 101: –6% 100: reserved	0x0
0	CON_LOOPBACK_1000BT_ENA	R/W	Set PHY into 1000BASE-T connector loopback mode. When enabled, the PHY only works with a connector loopback.	0x0

Table 192. LED Control—PHY_LED_CTRL (Address 0x1B) PHY Register

Bit	Name	Mode	Description	Default
15:12	LED_PIN3_MODE_CFG	R/W	Configures the functional mode of the LED Pin 3 output. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x8
11:8	LED_PIN2_MODE_CFG	R/W	Configures the functional mode of the LED Pin 2 output. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x6
7:4	LED_PIN1_MODE_CFG	R/W	Configures the functional mode of the LED Pin 1 output. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x1
3:0	LED_PIN0_MODE_CFG	R/W	Configures the functional mode of the LED Pin 0 output. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
For more information about the selectable LED functions, see "Parallel LED Output," page 55.				

Table 193. Auxiliary Control and Status—PHY_AUX_CTRL_STAT (Address 0x1C) PHY Register

Bit	Name	Mode	Description	Default
15	AUTONEG_COMPLETE	R/O	A read-only copy of PHY_STAT::AUTONEG_COMPLETE. Repeated here for convenience.	See note at end of table.
14	AUTONEG_STAT	R/O	When set, the auto-negotiation function is disabled in PHY_CTRL::AUTONEG_ENA.	0x0
13	NO_MDI_X_IND	R/O	When this field is set, the auto-negotiation state machine has determined that crossover does not exist in the signal path. This field is only valid after descrambler lock is achieved (see PHY_STAT_1000BT_EXT::DESCRAM_LOCKED) and automatic pair swap correction is enabled (see PHY_BYPASS_CTRL::PAIR_SWAP_DISABLE).	0x0
12	CD_PAIR_SWAP	R/O	When this field is set, the PHY has determined that the subchannel cable pairs C and D were swapped between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE).	0x0

Table 193. Auxiliary Control and Status—PHY_AUX_CTRL_STAT (Address 0x1C) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
11	A_POL_INVERSION	R/O	When set, this field indicates that the polarity of pair A was inverted between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE) and automatic polarity inversion is enabled (see PHY_BYPASS_CTRL::POL_INV_DIS). 1: Polarity is swapped on Pair A. 0: Polarity is not swapped on Pair A.	0x0
10	B_POL_INVERSION	R/O	When set, this field indicates that the polarity of pair B was inverted between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE) and automatic polarity inversion is enabled (see PHY_BYPASS_CTRL::POL_INV_DIS). 1: Polarity is swapped on Pair B. 0: Polarity is not swapped on Pair B.	0x0
9	C_POL_INVERSION	R/O	When set, this field indicates that the polarity of pair C was inverted between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE), in 1000BASE-T mode, and automatic polarity inversion is enabled (see PHY_BYPASS_CTRL::POL_INV_DIS). 1: Polarity is swapped on Pair C. 0: Polarity is not swapped on Pair C.	0x0
8	D_POL_INVERSION	R/O	When set, this field indicates that the polarity of pair D was inverted between the far-end transmitter and the receiver. In this case, the PHY corrects this internally. This field is only valid when auto-negotiation is complete (see AUTONEG_COMPLETE), in 1000BASE-T mode, and automatic polarity inversion is enabled (see PHY_BYPASS_CTRL::POL_INV_DIS). 1: Polarity is swapped on Pair D. 0: Polarity is not swapped on Pair D.	0x0
7	ACTIPHY_LINK_TIMER_MSB_CFG	RW	Most significant bit of the link status time-out timer. Together with ACTIPHY_LINK_TIMER_LSB_CFG, this field determines the duration from losing the link to when the ActiPHY enters low power state. For more information about the ActiPHY link status time-out timer, see “ActiPHY™ Power Management,” page 60. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	0x0
6	ACTIPHY_ENA	R/W	Enable ActiPHY power management mode. For more information about the ActiPHY mode, see “ActiPHY™ Power Management,” page 60. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA.	0x0

Table 193. Auxiliary Control and Status—PHY_AUX_CTRL_STAT (Address 0x1C) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
5	FDX_STAT	R/O	This field indicates the actual FDX/HDX operating mode of the PHY. 0: Half-duplex. 1: Full-duplex.	0x0
4:3	SPEED_STAT	R/O	This field indicates the actual operating speed of the PHY. 00: Speed is 10BASE-T. 01: Speed is 100BASE-TX. 10: Speed is 1000BASE-T. 11: Reserved.	0x0
2	ACTIPHY_LINK_TIMER_LSB_CFG	R/W	See ACTIPHY_LINK_TIMER_MSB_CFG.	0x1
1:0	ACTIPHY_SLEEP_TIMER_CFG	RW	This field controls the timer period the PHY stays in Low Power state before entering the LP Wake-up state. For more information about the ActiPHY sleep timer, see "ActiPHY™ Power Management," page 60. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	0x1
Copied fields have the same default values as their source fields.				

Table 194. Delay Skew Status—DELAY_SKEW_STAT (Address 0x1D)
PHY Register

Bit	Name	Mode	Description	Default
14:12	A_DELAY_SKEW	R/O	Indicates the additional delay (measured in integral symbol times) that is added internally at the pair A receiver input to align received symbols at pair A with the received symbols at the other pairs.	0x00
10:8	B_DELAY_SKEW	R/O	Indicates the additional delay (measured in integral symbol times) that added internally at the pair B receiver input to align received symbols at pair B with the received symbols at the other pairs.	0x00
6:4	C_DELAY_SKEW	R/O	Indicates the additional delay (measured in integral symbol times) that added internally at the pair C receiver input to align received symbols at pair C with the received symbols at the other pairs.	0x00
2:0	D_DELAY_SKEW	R/O	Indicates the additional delay (measured in integral symbol times) that added internally at the pair D receiver input to align received symbols at pair D with the received symbols at the other pairs.	0x00

Table 195. LED Behavior Control—PHY_LED_BEHAVIOR_CTRL (Address 0x1E) PHY Register

Bit	Name	Mode	Description	Default
15	RESERVED	R/W	Must be default value.	0x0
14	ALT_ACTIVITY_ENA	R/W	When set, the operation of the functional mode Activity changes and the Alternative Activity mode is defined. Activity changes from indicating both transmit and receive activity to indicating only transmit activity. Alternative Activity now indicates receive activity. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
13	RESERVED	R/W	Must be default value.	0x0
12	PULSING_ENA	R/W	Enable power-saving 5 kHz 20% duty-cycle pulsing of active LED pin outputs. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
11:10	BLINK_RATE_CFG	R/W	Configure blink rate of LEDs when applicable. If pulse stretching is selected rather than blink, this controls the stretch-period rather than the frequency. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). 00: 2.5 Hz / 400 ms 01: 5 Hz / 200 ms 10: 10 Hz / 100 ms 11: 20 Hz / 50 ms	0x1
9	RESERVED	R/W	Must be default value.	0x0
8:5	PULSE_STRETCH_ENA	R/W	Enable pulse-stretch behavior instead of blinking on per LED pin basis. MSB corresponds to MS LED and LSB corresponds to LS LED. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
4	RESERVED	R/W	Must be default value.	0x0
3:0	COMBINATION_DIS	R/W	Disable the blink combination for all the relevant LED pin functional modes. MSB corresponds to MS LED and LSB corresponds to LS LED. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0

Table 196. Memory Page Access—PHY_MEMORY_PAGE_ACCESS (Address 0x1F) PHY Register

Bit	Name	Mode	Description	Default
15:1	RESERVED	R/W	Setting this field to other values than the default may result in undefined behavior.	0x0000

Table 196. Memory Page Access—PHY_MEMORY_PAGE_ACCESS (Address 0x1F) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
0	PAGE_ACCESS_CFG	R/W	This bit controls the mapping of PHY registers 0x10 through 0x1E. When changing pages, all registers in the range 0x10 through 0x1E are replaced – even if the new memory-page does not define all addresses in the range 0x10 through 0x1E. 0: Register Page 0 is mapped (standard set). 1: Register Page 1 is mapped (extended set).	0x0

6.8.16 Extended Set PHY Registers

Set register 1F to 0x0001 to make the extended set of registers visible in the address range 0x10 through 0x1E. Set register 1F to 0x0000 to revert back to the standard register set.

Table 197. Extended Control Number 3—PHY_CTRL_EXT3 (Address 0x14)
PHY Register

Bit	Name	Mode	Description	Default
15:13	DACG_AMPLITUDE_1000BT_CFG	R/W	Fine control of the amplitude of the 1000BASE-T signal waveform. The signal level can be boosted or attenuated from the nominal setting to compensate for variations in characteristics of the magnetics so that the waveform on the media side of the transformer is compliant with the IEEE standard. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189, page 196). The allowed settings for these bits and the corresponding boost or attenuation amounts are: 011: +2% from hardware default, but equals switch software default 010: hardware default 001: –2% 000: –4% 111: –6% 110: –8% 101: –10% 100: reserved	0x2
12:9	RESERVED	R/O	Reserved.	0x00
8	RESERVED	R/W	Must be default value.	0x0
7:6	RESERVED	R/O	Reserved.	0x1
5	RESERVED	R/W	Must be default value.	0x0
4	SPEED_DOWNSHIFT_ENA	R/W	Enables automatic downshift of the auto-negotiation advertisement to the next lower available speed after the number of failed 1000BASE-T auto-negotiation attempts specified in SPEED_DOWNSHIFT_CFG. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189, page 196).	0x0

Table 197. Extended Control Number 3—PHY_CTRL_EXT3 (Address 0x14) *(continued)* PHY Register

Bit	Name	Mode	Description	Default
3:2	SPEED_DOWNSHIFT_CFG	R/W	Configures the number of unsuccessful 1000BASE-T auto-negotiation attempts that are required before the auto-negotiation advertisement is downshifted to the next lower available speed. This field applies only if automatic downshift of speed is enabled (see SPEED_DOWNSHIFT_ENA). This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189). 00: Downshift after 2 failed attempts. 01: Downshift after 3 failed attempts. 10: Downshift after 4 failed attempts. 11: Downshift after 5 failed attempts.	0x1
1	SPEED_DOWNSHIFT_STAT	R/O	This status field indicates that a downshift is required for the link to be established. If automatic downshifting is enabled (see SPEED_DOWNSHIFT_ENA), this is already done, that is, the current link speed is a result of a downshift.	0x0
0	RESERVED	R/O	Reserved.	0x0

Table 198. Extended Control Number 4—PHY_CTRL_EXT4 (Address 0x17) PHY Register

Bit	Name	Mode	Description	Default
15:11	PHY_ADDR	R/O	This field contains the PHY address of the current PHY port.	See note at end of table.
10	INLINE_POW_DET_ENA	R/W	Enables detection of inline powered device as part of the Auto Negotiation process. This is a sticky field; see PHY_CTRL_STAT_EXT::STICKY_RESET_ENA (Table 189).	0x0
9:8	INLINE_POW_DET_STAT	R/O	This field shows the status if a device is connected to the PHY that requires inline power. This field is only valid if inline powered device detection is enabled (see INLINE_DETECT_ENA) 00: Searching for devices. 01: Device found that requires inline power. 10: Device found that does not require inline power. 11: Reserved.	0x0
7:0	CRC_1000BT_CNT	R/O	This field indicates how many packets are received that contain a CRC error. This field is cleared on read and saturates at all-ones. This field is only valid in 1000BASE-T mode.	0x00
The reset value of the address field corresponds to the PHY in which it resides.				

Table 199. VeriPHY Control—PHY_VERIPHY_CTRL (Address 0x18) PHY Register

Bit	Name	Mode	Description	Default
15	VERIPHY_TRIGGER	R/W	Set to trigger a VeriPHY operation. This field is cleared by hardware when acknowledged.	0x0
14	VERIPHY_RES_VALID	R/O	This field indicates if VeriPHY results are valid.	0x0
13:0	RESERVED	R/O	Reserved.	0x0000

Table 200. 1000BASE-T EPG Number 1—PHY_1000BT_EPG1 (Address 0x1D) PHY Register

Bit	Name	Mode	Description	Default
15	EPG_ENA	R/W	Enables the Ethernet packet generator. When this field is set, the EPG is selected as the driving source for the PHY transmit signals, and the MAC transmit pins are disabled.	0x0
14	EPG_RUN_ENA	R/W	Begin transmission of Ethernet packets. Clear to stop the transmission of packets. If a transmission is in progress, the transmission of packets is stopped after the current packet is transmitted. This field is valid only when the EPG is enabled (see EPG_ENA).	0x0
13	TRANSMIT_DURATION_CFG	R/W	Configure the duration of the packet generation. When set, the EPG continuously transmits packets as long as the field EPG_RUN_ENA is set. When cleared, the EPG transmits 30,000,000 packets when the field EPG_RUN_ENA is set, after which time, field EPG_RUN_ENA is automatically cleared. This field is latched when packet generation begins, that is, setting EPG_RUN_ENA in this register.	0x0
12:11	PACKET_LEN_CFG	R/W	This field selects the length of packets to be generated by the EPG. This field is latched when packet generation begins, that is, setting EPG_RUN_ENA in this register. 00: 125 byte packets 01: 64 byte packets 10: 1518 byte packets 11: 10,000 byte packets	0x0
10	INTER_PACKET_GAP_CFG	R/W	This field configures the inter-packet gap for packets generated by the EPG. This field is latched when packet generation begins, that is, setting EPG_RUN_ENA in this register. 0: 96 ns inter-packet gap 1: 8,192 ns inter-packet gap	0x0
9:6	DEST_ADDR_CFG	R/W	This field configures the low nibble of the most significant byte of the destination MAC address. The rest of the destination MAC address is all-ones. For example, setting this field 0x2 results in packets generated with a destination address of 0xF2FFFFFFFFFF. This field is latched when packet generation begins, that is, setting EPG_RUN_ENA in this register.	0x1

Table 200. 1000BASE-T EPG Number 1—PHY_1000BT_EPG1 (Address 0x1D) *(continued)*
PHY Register

Bit	Name	Mode	Description	Default
5:2	SRC_ADDR_CFG	R/W	This field configures the low nibble of the most significant byte of the source MAC address. The rest of the source MAC address is all-ones. For example, setting this field 0xE results in packets generated with a source address of 0xFEFFFFFFFFFF. This field is latched when packet generation begins, that is, setting EPG_RUN_ENA in this register.	0x0
1	RESERVED	R/O	Reserved.	0x0
0	BAD_FCS_ENA	R/W	When this field is set, the EPG generates packets containing an invalid Frame Check Sequence (FCS). When cleared, the EPG generates a packet with valid FCS. This field is latched when packet generation begins, that is, setting EPG_RUN_ENA in this register.	0x0

Table 201. 1000BASE-T EPG Number 2—PHY_1000BT_EPG2 (Address 0x1E)
PHY Register

Bit	Name	Mode	Description	Default
15:0	PACKET_PAYLOAD_CFG	R/W	Each packet generated by the EPG contains a repeating sequence of this field as payload. This field is latched when packet generation begins, that is,setting PHY_1000BT_EPG1::EPG_RUN_ENA (Table 200).	0x0000

6.9 SFR Register Details

The registers in this section are only accessible from the V-Core CPU.

6.9.1 General-Purpose I/O SFRs

This group of registers provides access to the V-Core CPU's GPIO bits. The GPIO registers are only available if the ICPU_PI_En pin is strapped high, that is, if the V-Core CPU has access to the parallel interface pins.

Table 202. General-Purpose I/O Input—GPIO_IN (Address 0x80)

Bit	Name	Mode	Description	Default
1	GI1	R/O	The value of this bit reflects the value of the V-Core CPU's GPIO pin number 1. When the GPIO for this bit is configured as an output bit, the read value becomes the value of the corresponding output.	0x0
0	GI0	R/O	See GI1 for a description. This bit is also connected to external interrupt number 1.	0x0

Table 203. General-Purpose I/O Output—GPIO_OUT (Address 0x90)

Bit	Name	Mode	Description	Default
1	GO1	R/W	The value of this bit is presented on the V-Core CPU's GPIO pin number 1 when the bit in question is configured as an output (for more information, see "General-Purpose I/O Output Enable—GPIO_OE (Address 0xA0)," page 208).	0x0
0	GO0	R/W	See GO1 for a description.	0x0

Table 204. General-Purpose I/O Output Enable—GPIO_OE (Address 0xA0)

Bit	Name	Mode	Description	Default
1	GOE1	R/W	Setting this bit enables the device's 8051 GPIO pin number 1 for output. The value specified in the GPIO_OUT::GO1 bit is presented on the pin. When this bit is cleared, the pin is configured as an input pin. 0: Configure 8051 GPIO pin as input (as seen from the device). 1: Configure 8051 GPIO pin as output (as seen from the device).	0x0
0	GOE0	R/W	See GOE1 for a description.	0x0

Table 205. General-Purpose I/O Status—GPIO_STAT (Address 0xA1)

Bit	Name	Mode	Description	Default
1	GS1	R/W	Whenever GPIO_IN::GI1 changes, this bit gets set. The bit is sticky in the sense that it keeps its value after it is set. The bit is cleared by writing a 1 to it. Note that this field also senses changes on GPIO_OUT::GO1 when the pin is configured as an output. 0: There have been no events on this GPIO pin. 1: There was at least one event on this GPIO pin.	0x0
0	GS0	R/W	See GS1 for a description.	0x0

6.9.2 Dual-Data Pointer SFRs

The V-Core CPU employs dual-data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The V-Core CPU maintains the standard data pointer as DPTR0 at SFR locations 0x82 and 0x83. The V-Core CPU adds a second data pointer (DPTR1) at SFR locations 0x84 and 0x85 and a select register at 0x86 as described below.

Table 206. Data Pointer 1 Low—DPL1 (Address 0x84)

Bit	Name	Mode	Description	Default
7:0	VALUE	R/W	Access this register to read or write the value of the least significant byte of DPTR1. This register is used in external data accesses when the DPS::SEL bit is 1.	0x00

Table 207. Data Pointer 1 High—DPH1 (Address 0x85)

Bit	Name	Mode	Description	Default
7:0	VALUE	R/W	Access this register to read or write the value of the most significant of DPTR1. This register is used in external data accesses when the DPS::SEL bit is 1.	0x00

Table 208. Data Pointer Select—DPS (Address 0x86)

Bit	Name	Mode	Description	Default
0	SEL	R/W	When this bit is 0, instructions that use the DPTR, also use DPL0 and DPH0. When this bit is 1, instructions that use the DPTR, also use DPL1 and DPH1. Because no other bits in this SFR are used, the fastest way to toggle this bit is to issue an INC DPS instruction.	0x0

6.9.3 Memory Access Control SFRs

This group of SFRs provides control over the accessed memory.

Table 209. Special Function Register—SPC_FNC (Address 0x8F)

Bit	Name	Mode	Description	Default
0	WRS	R/W	External ROM is normally read-only, but for program downloading, you can set this bit for writing. This causes all MOVX @DPTR-like instructions to activate the ICPU_ROM_nCS signal rather than the ICPU_RAM_nCS signal on the external memory bus. 0: When writing to external memory, activate ICPU_RAM_nCS signal. 1: When writing to external memory, activate ICPU_ROM_nCS signal.	0x0

Table 210. Paging Control—PG (Address 0xB0)

Bit	Name	Mode	Description	Default
7:4	IFP	R/W	Instruction fetch page bits. These four page bits are presented on the address bus (ICPU_Addr[19:16]) when an instruction fetch is in progress, that is, when both ICPU_ROM_nCS and ICPU_nRD are asserted. **Note** This is also the case when the code is read programmatically with MOVC instructions.	0x0
3:0	OP	R/W	Page bits for any other type of memory access. These four page bits are presented on the address bus (ICPU_Addr[19:16]) when the access is *not* an instruction fetch (see also PG::IFP in this register).	0x0
The paging bits are used to extend the 8051's 16-bit address space to a 20-bit address bus, allowing for access to up to one megabyte of external data and code. You programmatically select the page to target by changing the value of the bits in this register. These bits map directly to the ICPU_Addr[19:16] bits. The paging bits are only available if the ICPU_PI_En pin is strapped high, that is, if the V-Core CPU has access to the parallel interface.				

Table 211. Access External Flash as External RAM—SPC_FNC2 (Address 0xF1)

Bit	Name	Mode	Description	Default
0	ENA	R/W	When this bit is set, all external RAM accesses are forwarded to external ROM. This is useful in cases where a program executes from one page in flash, and the program wishes to programmatically read another page in flash. The program sets the PG::IFP to point to the page where the program executes, and the PG::OP paging bits point to the page in flash from which data should be read. Then the program sets the SPC_FNC2::ENA bit and reads from external RAM using MOVX instructions. These instructions cause a flash read using the PG::OP paging bits.	0x0

6.9.4 Frame Present SFRs

This group of registers is connected to the CPU Capture RAM.

Table 212. Enable CPU Capture RAM Interrupts—FPIE (Address 0xA9)

Bit	Name	Mode	Description	Default
1	Q1	R/W	Set this bit to enable interrupts on the external interrupt number 0 of the V-Core CPU whenever a frame is present in the Capture RAM queue number 1. To get the interrupt through to the program, both this bit and the SFR::IE::EX0 and SFR::IE:EA bits must be set.	0x0
0	Q0	R/W	Set this bit to enable interrupt on the external interrupt number 0 of the V-Core CPU whenever a frame is present in the Capture RAM queue number 0. To get the interrupt through to the program, both this bit and the SFR::IE::EX0 and SFR::IE:EA bits must be set.	0x0

Table 213. CPU Capture RAM Frame Present Status—FPSTAT (Address 0xAA)

Bit	Name	Mode	Description	Default
1	Q1	R/O	This bit is set whenever at least one frame is present in the Capture RAM queue number 1.	0x0
0	Q0	R/O	This bit is set whenever at least one frame is present in the Capture RAM queue number 0.	0x0

6.9.5 Watchdog SFRs

This group of registers provides control over the built-in watchdog.

Table 214. Watchdog Data—WDDA (Address 0xA2)

Bit	Name	Mode	Description	Default
7:0	DATA	R/W	Alternately write the two values 0xBE and 0xEF to this register to reset the watchdog's 1.718 seconds interval timer. After enabling the watchdog (see the WDCON register – Table 215), the first value written to this field must be 0xBE. When read, the register returns the latest written value. Failing to write the correct value results in an 8051 reset. Failing to write the correct value within 1.718 seconds after the previous write also causes an 8051 reset. A reset caused by the watchdog can be determined by reading the ICPU_CTRL::WATCHDOG_RST bit in the SYSTEM registers block, which is not reset with an 8051 reset.	0xEF

Table 215. Watchdog Control—WDCON (Address 0xA3)

Bit	Name	Mode	Description	Default
0	WD_EN	R/W	Write a 1 to this field to enable the watchdog. Doing so also resets the watchdog timer. The next byte to be written to WDDA is 0xBE. Write a 0 to this field to disable the watchdog.	0x0

6.9.6 Additional Timer-Related SFRs

The third timer (Timer 2) is controlled through these SFRs, as are the Timer 0 and Timer 1's count incrementers. The additional timer also affects the layout of the Interrupt Enable (IE) and Interrupt Priority (IP) registers, whose extra bits are described within here.

Table 216. Timer Clock and External Memory Stretch Cycles Control—CKCON (Address 0x8E)

Bit	Name	Mode	Description	Default
5	T2M	R/W	Timer 2 clock select. Selects whether Timer 2 increments every 4 or 12 V-Core CPU clock cycles. The value of this bit has no effect when Timer 2 is used for baud-rate generation. 0: Timer 2 increments every 12 V-Core CPU clock cycles. 1: Timer 2 increments every 4 V-Core CPU clock cycles.	0x0
4	T1M	R/W	Timer 1 clock select. Selects whether Timer 1 increments every 4 or 12 V-Core CPU clock cycles. 0: Timer 1 increments every 12 V-Core CPU clock cycles. 1: Timer 1 increments every 4 V-Core CPU clock cycles.	0x0
3	T0M	R/W	Timer 0 clock select. Selects whether Timer 0 increments every 4 or 12 V-Core CPU clock cycles. 0: Timer 0 increments every 12 V-Core CPU clock cycles. 1: Timer 0 increments every 4 V-Core CPU clock cycles.	0x0
2:0	MD	R/W	Controls memory stretch cycles. Controls the number of cycles to be used for external MOVX instructions. All types of external accesses except instruction fetches and MOVC instructions are affected by this field. The ICPU_nRD, ICPU_nWR, ICPU_RAM_nCS, and ICPU_ROM_nCS signals are affected by the value of this field. 000: Width is 2 V-Core CPU clock cycles. 001: Width is 4 V-Core CPU clock cycles. 010: Width is 8 V-Core CPU clock cycles. ... 111: Width is 28 V-Core CPU clock cycles.	0x1

Table 217. Interrupt Enable—IE (Address 0xA8)

Bit	Name	Mode	Description	Default
7	EA	R/W	Global interrupt enable. See standard 8051 documentation.	0x0
6	Reserved	R/W		0x0
5	ET2	R/W	Enable Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable Timer 2 interrupt generated by T2CON::TF2 flag.	0x0

Table 217. Interrupt Enable—IE (Address 0xA8) *(continued)*

Bit	Name	Mode	Description	Default
4	ES	R/W	Enable serial port interrupt. See standard 8051 documentation.	0x0
3	ET1	R/W	Enable Timer 1 interrupt. See standard 8051 documentation.	0x0
2	EX1	R/W	Enable External interrupt 1. See standard 8051 documentation.	0x0
1	ET0	R/W	Enable Timer 0 interrupt. See standard 8051 documentation.	0x0
0	EX0	R/W	Enable External interrupt 0. See standard 8051 documentation.	0x0

Table 218. Interrupt Priority—IP (Address 0xB8)

Bit	Name	Mode	Description	Default
7	Reserved	R/W		0x1
6	Reserved	R/W		0x0
5	PT2	R/W	Timer 2 interrupt priority control. 0: Sets Timer 2 interrupt (T2CON::TF2) to low priority. 1: Sets Timer 2 interrupt (T2CON::TF2) to high priority.	0x0
4	PS	R/W	See standard 8051 documentation.	0x0
3	PT1	R/W	See standard 8051 documentation.	0x0
2	PX1	R/W	See standard 8051 documentation.	0x0
1	PT0	R/W	See standard 8051 documentation.	0x0
0	PX0	R/W	See standard 8051 documentation.	0x0

Table 219. Timer 2 Control—T2CON (Address 0xC8)

Bit	Name	Mode	Description	Default
7	TF2	R/W	Timer 2 overflow flag. Hardware sets TF2 when Timer 2 overflows from 0xFFFF. TF2 must be cleared to 0 by the software. TF2 is only set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.	0x0
6	Reserved	R/W	Always write a 0 to this bit. Writing a 1 may cause unpredicted behavior.	0x0
5	RCLK	R/W	Receive clock flag. Determines whether Timer 1 or Timer 2 is used for the serial port timing of received data in serial mode 1 or 3. 0: Selects Timer 1 overflow as the receive clock. 1: Selects Timer 2 overflow as the receive clock.	0x0

Table 219. Timer 2 Control—T2CON (Address 0xC8) *(continued)*

Bit	Name	Mode	Description	Default
4	TCLK	R/W	Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for the serial port timing of transmitted data in serial mode 1 or 3. 0: Selects Timer 1 overflow as the transmit clock. 1: Selects Timer 2 overflow as the transmit clock.	0x0
3	Reserved	R/W	Always write a 0 to this bit. Writing a 1 may cause unpredicted behavior.	0x0
2	TR2	R/W	Timer 2 run control flag. 0: Stops Timer 2. 1: Starts Timer 2.	0x0
1	Reserved	R/W	Always write a 0 to this bit. Writing a 1 may cause unpredicted behavior.	0x0
0	Reserved	R/W	Always write a 0 to this bit. Writing a 1 may cause unpredicted behavior.	0x0

Table 220. Timer 2 Capture Low—RCAP2L (Address 0xCA)

Bit	Name	Mode	Description	Default
7:0	VALUE	R/W	Least significant byte of reload-value when Timer 2 overflows.	0x00

Table 221. Timer 2 Capture High—RCAP2H (Address 0xCB)

Bit	Name	Mode	Description	Default
7:0	VALUE	R/W	Most significant byte of reload-value when Timer 2 overflows.	0x00

Table 222. Timer 2 Low—TL2 (Address 0xCC)

Bit	Name	Mode	Description	Default
7:0	VALUE	R/W	Least significant byte of the current value of the 16-bit count.	0x00

Table 223. Timer 2 High—TH2 (Address 0xCD)

Bit	Name	Mode	Description	Default
7:0	VALUE	R/W	Most significant byte of the current value of the 16-bit count.	0x00

6.9.7 Chip Register Access SFRs

This group of registers provides access to the chip's internal registers.

Table 224. Register Access Done—RA_DONE (Address 0xF8)

Bit	Name	Mode	Description	Default
0	DONE	R/W	When this bit is set, a transaction (read or write) to the chip's registers is complete. The bit is cleared when either of the data byte registers (RA_DA0-3 below) is read, a new request is submitted, or whenever a 1 is written to the bit. Note that after a chip-reset, it is necessary to clear the hardware state machine by writing a 1 to this bit.	0x0

Table 225. Register Access Block and Subblock—RA_BLK (Address 0xF9)

Bit	Name	Mode	Description	Default
7:5	BLOCK	R/W	The ID of the block of the chip to access.	0x0
3:0	SUBBLOCK	R/W	The subblock number of the chip to access.	0x0

Table 226. Register Access Read Address—RA_AD_RD (Address 0xFA)

Bit	Name	Mode	Description	Default
7:0	ADDR	R/W	Address within the block and subblock specified in RA_BLK to read. Writing to this field initiates a read of a register. Keep polling the RA_DONE::DONE field and wait for it to become 1, then read the returned data from the RA_DAx registers.	0x00

Table 227. Register Access Write Address—RA_AD_WR (Address 0xFB)

Bit	Name	Mode	Description	Default
7:0	ADDR	R/W	Address within the block/subblock specified with RA_BLK to write to. Writing to this field initiates a write to the register with address ADDR. The data to write should be set up beforehand by writing to the RA_DAx registers.	0x00

Table 228. Register Access Data Byte Number 0—RA_DA0 (Address 0xFC)

Bit	Name	Mode	Description	Default
7:0	DATA	R/W	Read this register to obtain bits 7:0 of the 32-bit data returned from a read, or write bits 7:0 of the 32-bit data to write to a particular chip register. In addition to returning data, reading this field also clears the RA_DONE::DONE bit.	0x00

Table 229. Register Access Data Byte Number 1—RA_DA1 (Address 0xFD)

Bit	Name	Mode	Description	Default
7:0	DATA	R/W	Read this register to obtain bits 15:8 of the 32-bit data returned from a read, or write bits 15:8 of the 32-bit data to write to a particular register. In addition to returning data, reading this field also clears the RA_DONE::DONE bit.	0x00

Table 230. Register Access Data Byte Number 2—RA_DA2 (Address 0xFE)

Bit	Name	Mode	Description	Default
7:0	DATA	R/W	Read this register to obtain bits 23:16 of the 32-bit data returned from a read, or write bits 23:16 of the 32-bit data to write to a particular register. In addition to returning data, reading this field also clears the RA_DONE::DONE bit.	0x00

Table 231. Register Access Data Byte Number 3—RA_DA3 (Address 0xFF)

Bit	Name	Mode	Description	Default
7:0	DATA	R/W	Read this register to obtain bits 31:24 of the 32-bit data returned from a read, or write bits 31:24 of the 32-bit data to write to a particular register. In addition to returning data, reading this field also clears the RA_DONE::DONE bit.	0x00

6.9.8 Other SFRs

Table 232. Program Status Word—PSW (Address 0xD0)

Bit	Name	Mode	Description	Default
7	CY	R/W	See standard 8051 documentation.	0x0
6	AC	R/W	See standard 8051 documentation.	0x0
5	F0	R/W	See standard 8051 documentation.	0x0
4	RS1	R/W	See standard 8051 documentation.	0x0
3	RS0	R/W	See standard 8051 documentation.	0x0
2	OV	R/W	See standard 8051 documentation.	0x0
1	F1	R/W	User Flag 1. Bit-addressable, general-purpose flag for software control.	0x0
0	P	R/O	See standard 8051 documentation.	0x0

7 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC7395 device.

7.1 DC Characteristics

This section provides the DC specifications for the VSC7395 device.

Specific inputs on the SparX-G5e have built-in pull resistors to ease hardware design and reduce overall system cost or to meet a specific standard requirement. For more information about the signals with a built-in pull resistor, see "Pins by Function," page 252.

Table 233. Built-in Pull Resistor Specifications

Symbol	Parameter	Minimum	Maximum	Unit
R_{PU}	Built-in pull-up resistor	75	125	kΩ
R_{PD}	Built-in pull-down resistor	75	125	kΩ

7.1.1 DC Specifications for the Reference Clock

The following table shows the DC specifications for RefClk.

Table 234. DC Specifications for RefClk

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage	2.1			V
V_{IL}	Input low voltage			0.8	V
I_{IH}	Input high current			5	µA
I_{IL}	Input low current	–5			µA
C_I	Input capacitance		3		pF

7.1.2 DC Specifications for RGMII and MII-M Using 2.5 V Power Supply

The outputs and inputs of the RGMII and MII Management interfaces meet or exceed the requirements in the JEDEC standard JESD8-5 2.5 V CMOS interfaces. All RGMII outputs and inputs comply with the specifications listed in the following table.

Table 235. DC Specifications for RGMII and MII-M Using 2.5 V Power Supply

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
		Supply	Input/Output				
V_{OH}	Output high voltage	V_{DD_IOMAC} = minimum	I_{OH} = –1.0 mA	2.0			V
V_{OL}	Output low voltage	V_{DD_IOMAC} = maximum	I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input high voltage			1.7		3.0	V
V_{IL}	Input low voltage			–0.3		0.7	V
I_{IH}	Input high current (1)		$V_I = V_{DD\_IOMAC}$			5	µA
I_{IL}	Input low current (1)		V_I = 0.0 V	–5			µA
C_I	Input capacitance				3		pF

1. Input high current and input low current equal maximum leakage current, excluding current in built-in pull resistor.

7.1.3 DC Specifications for MII and GMII Using 3.3 V Power Supply

The outputs and inputs of the MII and GMII interfaces have been designed to meet or exceed the requirements of IEEE Std 802.3-2002 for the MII (Clause 22.4) and GMII (Clause 35.4), except for the 5 V tolerance.

All MII and GMII outputs and inputs comply with the specifications in the following table.

Table 236. DC Specifications for MII and GMII Using 3.3 V Power Supply

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
		Supply	Input/Output				
V_{OH}	Output high voltage	V_{DD_IOMAC} = minimum	I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output low voltage	V_{DD_IOMAC} = maximum	I_{OL} = 4.0 mA			0.40	V
V_{IH}	Input high voltage			2.0		V_{DD_IOMAC} + 0.3	V
V_{IL}	Input low voltage					0.90	V
I_{IH}	Input high current (1)		$V_I = V_{DD\_IOMAC}$			5	µA
I_{IL}	Input low current (1)		V_I = 0.0 V	–5			µA
C_I	Input capacitance				3		pF

1. Input high current and input low current equal maximum leakage current, excluding current in built-in pull resistors.

7.1.4 DC Specifications for MII Management Using 3.3 V Power Supply

The outputs and inputs of the MII Management interfaces have been designed to meet or exceed the requirements of IEEE Std 802.3-2002 for the MII (Clause 22.4), except for the 5 V tolerance.

All MII Management outputs and inputs comply with the specifications in the following table.

Table 237. DC Specifications for MII Management Using 3.3 V Power Supply

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
		Supply	Input/Output				
V_{OH}	Output high voltage	V_{DD_IOMAC} = minimum	I_{OH} = –4.0 mA	2.4			V
V_{OL}	Output low voltage	V_{DD_IOMAC} = maximum	I_{OL} = 4.0 mA			0.40	V
V_{IH}	Input high voltage			2.0		V_{DD_IOMAC} + 0.3	V
V_{IL}	Input low voltage					0.80	V
I_{IH}	Input high current (1)		$V_I = V_{DD\_IOMAC}$			5	µA
I_{IL}	Input low current (1)		V_I = 0.0 V	–5			µA
C_I	Input capacitance				3		pF

1. Input high current and input low current equal maximum leakage current, excluding current in built-in pull resistors.

7.1.5 DC Specifications for PI, V-Core CPU, SI, JTAG, and Other Control Signals

The following I/O signals comply with the specifications in Table 238.

PI_Addr[16:0]	SI_Clk	JTAG_nTRST	ICPU_RxD	Clk125_En
PI_Data[7:0]	SI_DI	JTAG_TMS	ICPU_TxD	Osc_En
PI_IRQ[1:0]	SI_DO	JTAG_TDO	ICPU_SI_Boot_En	GPIO_[3:0]
PI_nCS	SI_nEn	JTAG_TCK	ICPU_PI_En	nReset
PI_nDone		JTAG_TDI	ICPU_Addr[19:16]	Reserved_[4:3]
PI_nOE				Test_Code[2:0]
PI_nWR				

Table 238. DC Specifications for PI, V-Core CPU, SI, JTAG, and Other Control Signals

Symbol	Parameter	Condition		Minimum	Typical	Maximum	Unit
		Supply	Input/Output				
V_{OH}	Output high voltage	V_{DD_IOCPU} = minimum	I_{OH} = –100 µA	V_{DD_IOCPU} – 0.2			V
			I_{OH} = –2 mA	2.4			V
V_{OL}	Output low voltage	V_{DD_IOCPU} = maximum	I_{OL} = 100 µA			0.2	V
			I_{OL} = 2 mA			0.4	V
I_{OH}	Output high current					–10	mA
I_{OL}	Output low current					10	mA
V_{IH}	Input high voltage			2.1		3.6 (1)	V
V_{IL}	Input low voltage			–0.3		0.8	V
I_{IH}	Input high current (2)		$V_I = V_{DD\_IOCPU}$			5	µA
I_{IL}	Input low current (2)		V_I = 0.0 V	–5			µA
I_{OZ}	Output high-Z current (2)		0 V ≤ V_I ≤ V_{DD_IOCPU}			5	µA
C_I	Input capacitance				3		pF

1. V_{IH}(max) = 5.5 V for JTAG input signals.
2. Input high current and input low current and output high-Z current equal maximum leakage current, excluding current in built-in pull resistors

For more information about the GPIO_x pin current capabilities, see "GPIO," page 286.

7.1.6 DC Specifications for LED Interface Signals

The LED outputs are designed to drive light emitting diodes directly from the outputs.

Table 239. DC Specifications for LED Interface Signals

Symbol	Parameter	Condition		Minimum	Maximum	Unit
		Supply	Input/Output			
V_{OH}	Output high voltage	V_{DD_A33} = minimum	I_{OH} = –2 mA	2.4		V
V_{OL}	Output low voltage	V_{DD_A33} = maximum	I_{OL} = 2 mA		0.4	V
I_{OL}	Output low current				18	mA
I_{OH}	Output high current			–18		mA
I_{OZ}	Output high-Z current (1)		0 V ≤ V_I ≤ V_{DD_A33}		5	µA

1. Output high-Z current equals maximum leakage current, excluding current in built-in pull resistors.

7.2 Current Consumption

The following table shows the absolute maximum operating current for the SparX-G5e device.

Note Mode of operation affects the maximum operating current. Not all power domains consume maximum power at the same time. For information about the maximum power consumption, see Table 242, page 222.

Table 240. Maximum Operating Current

Symbol	Parameter	Condition	Maximum	Unit
I_{DD}	Operating current for core	V_{DD} = maximum	1.00	A
I_{DD_IOCPU}	Operating current for V_{DD_IOCPU}	V_{DD_IOCPU} = maximum	30	mA
I_{DD_IOMAC}	Operating current for V_{DD_IOMAC}, 2.5 V	V_{DD_IOMAC} = maximum, running RGMII full load 1518-byte packets with 0x0F0F data	65	mA
	Operating current for V_{DD_IOMAC}, 3.3 V	V_{DD_IOMAC} = maximum, running GMII full load 1518-byte packets with 0x00FF data	80	mA
I_{DD_A12}	Operating current for 1.2 V analog outputs	V_{DD_A12} = maximum	0.25	A
I_{DD_A33}	Operating current for 3.3 V analog outputs	V_{DD_A33} = maximum	0.77	A
Note All power consumption figures assume 100% Tx activity.				

7.2.1 Typical Current Consumption

The following table shows typical values for current consumption for the SparX-G5e device in various situations. The values are measured under typical conditions (process, temperature, and supply voltage).

Table 241. Typical Current Consumption

Supply	Idle	Full[1]	Unit
V_{DD} (1.2 V)	0.70	0.80	A
V_{DD_IOCPU} (3.3 V)	5	5	mA
V_{DD_IOMAC} (3.3 V / 2.5 V)	5	6	mA
V_{DD_A12} (1.2 V)	0.18	0.18	A
V_{DD_A33} (3.3 V)	0.56	0.56	A
Note All power consumption values assume 100% Tx activity.			

1. Full traffic on all 1-Gbps ports and the parallel CPU interface.

7.2.2 Power Consumption

The following table shows the typical and maximum power consumption based on the currents and supply voltages listed in Table 240 and Table 241.

Table 242. Power Consumption

Parameter	Value	Unit
Maximum power consumption	4.4	W
Typical power consumption (1)	3.1	W

1. Full traffic on all 1-Gbps ports.

7.3 AC Characteristics

All AC electrical characteristics are guaranteed over worst-case to best-case silicon, recommended operating temperature, recommended power supply voltages, and under the individual load conditions given in the following sections.

7.3.1 AC Specifications for the Reference Clock

The SparX-G5e system clock can be provided either by the RefClk or by an external crystal using the Xtal1 and Xtal2 pins.

7.3.1.1 AC Specifications for the RefClk Option

The signal applied to the RefClk input must comply with the requirements in the following table at the pin of the SparX-G5e device.

Table 243. AC Specifications for RefClk

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f	Nominal frequency	25-MHz RefClk		25		MHz
		125-MHz RefClk		125		MHz
	RefClk frequency tolerance	See note 1.	–100 (2)		100 (2)	ppm
	Clock duty cycle	V_{DD_A33} / 2	40	50	60	%
	Total jitter (peak-to-peak)				300	ps
t_r, t_f	Rise time and fall time	25-MHz RefClk, 0.8 V to 2.0 V			4	ns
		125-MHz RefClk, 0.8 V to 2.0 V			1	ns

1. Total frequency offset tolerance including initial offset, stability over temperature, and aging.
2. Except for RGMII mode, which is ±50 ppm.

7.3.1.2 AC Specifications for the Crystal Option

The crystal must comply with the requirements in the following table.

Table 244. AC Specifications for the Crystal Option

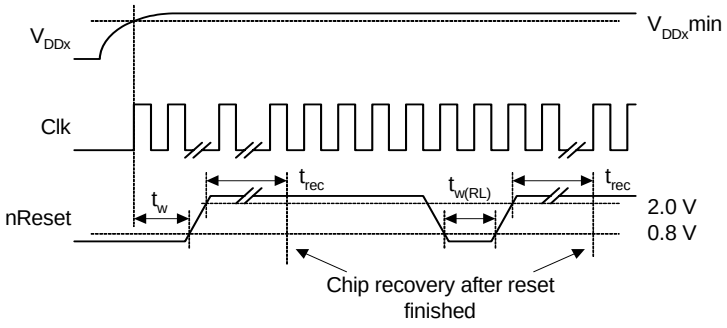
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f	Nominal frequency	25-MHz crystal option (1)		25		MHz
	Xtal frequency tolerance	See note 2.	–90 (3)		90 (3)	ppm
C_L	Crystal parallel load capacitance		18		20	pF
ESR	Equivalent series resistance of crystal			10	30	Ω

1. Fundamental mode, AT-cut type, parallel resonant crystal.
2. Total frequency offset tolerance including initial offset, stability over temperature, aging, and capacitive loading.
3. Except for RGMII mode, which is ±40 ppm.

7.3.2 Reset Timing

The following figure shows the nReset signal waveform and required measurement points for the timing specification.

Figure 34. nReset Signal Timing Parameters



The nReset assertion time during power-up is measured from when the later of the following conditions occur:

- Power supplies have reached within valid levels plus the clock signal is stable.
- nReset signal enters the transition region.

The signal applied to the nReset input must comply with the specifications listed in the following table at the reset pin of the SparX-G5e device.

Table 245. AC Specifications for nReset

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_w	nReset assertion time after power supplies and clock stabilize		20		ns
t_{rec}	Recovery time from reset inactive to device fully active			20	ms
$t_w(RL)$	Reset pulse width		20		ns
t_r, t_f	Rise time and fall time of nReset	0.8 V to 2.0 V		10	ns

7.3.3 AC Specifications for RGMII (10/100/1000 Mbps)

All AC specifications for the RGMII meet or exceed the requirements of the HP RGMII draft 1.3.

The RGMII timing parameters are defined in the figures in this section.

The skew between the clock and the other signals (both Tx and Rx) is defined as the time period between when the signals and when the clock reach the threshold value of 1.25 V. This is a double-data rate interface, so both the rising and falling edge of the clock is used.

The following figures show the RGMII transmit and receive waveforms and required measurement points for the different signals. All AC timing requirements are specified relative to 1.25 V. Measurements are made at the measurement point shown in Figure 39.

The RGMII can operate in either a standard mode or a compensated mode, where the required alignment between clock and data is performed internally in the switch.

In timing compensated mode, GMIIx_GTXDELAY and GMIIx_RXDELAY are set to 11.

Figure 35. RGMII Transmit Timing Diagram

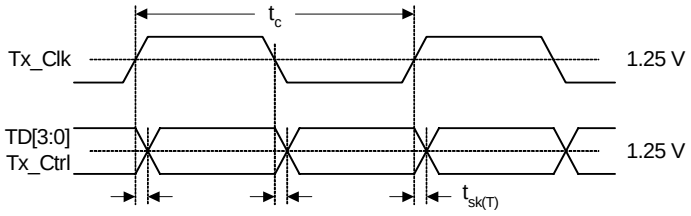


Figure 36. RGMII Transmit Timing Diagram, Compensated

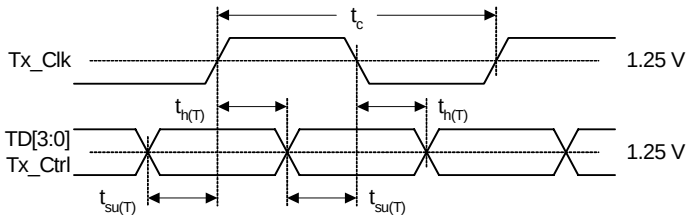


Figure 37. RGMII Receive Timing Diagram

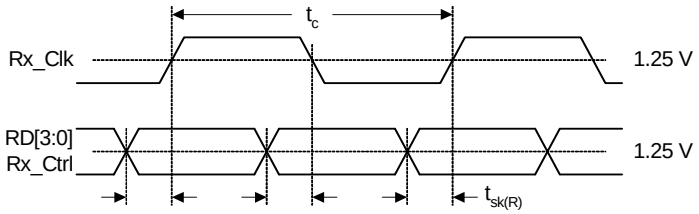
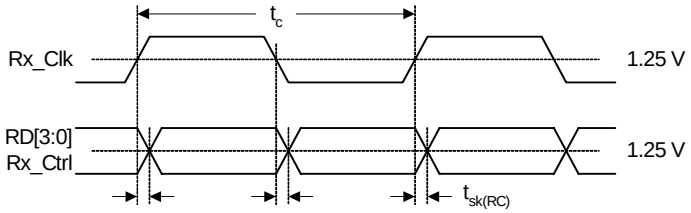


Figure 38. RGMII Receive Timing Diagram, Compensated



Additionally, in 10/100 RGMII mode, data is duplicated on the falling edge of the clock (no data transitions on the falling clock).

All RGMII transmit signals comply with the specifications in the following two tables when measured using the test circuit in Figure 39. All RGMII receive signal requirements are requested at the pins of the SparX-G5e device.

Table 246. AC Specifications for RGMII 1000 Mbps

Symbol	Parameter	Condition	Minimum	Typical (1)	Maximum	Unit
f	Clock frequency	1000 Mbps		125		MHz
	Clock frequency stability		–50		50	ppm
t_c	Clock cycle time	1.25 V	7.2	8	8.8	ns
	Clock duty cycle	1.25 V	45	50	55	%
t_r	RGMII signal rise time	20% to 80% (2)			0.75	ns
t_f	RGMII signal fall time	80% to 20% (2)			0.75	ns
$t_{sk(T)}$	Data to clock output skew	1.25 V	–500	0	500	ps
$t_{sk(R)}$	Data to clock input skew (3)	1.25 V	1		2.6	ns
$t_{su(T)}$	Data setup to clock in compensated mode	1.25 V	1.2	2.0		ns
$t_{h(T)}$	Data hold from clock in compensated mode	1.25 V	1.2	2.0		ns
$t_{sk(RC)}$	Data to clock input skew in compensated mode	1.25 V	–1		0.6	ns

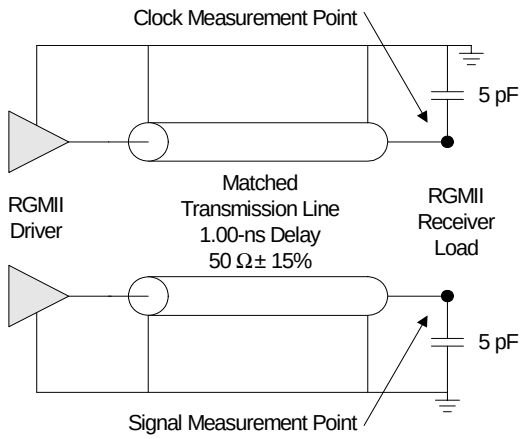
1. Typical values are at 25°C.
2. Measured relative to worst-case DC output levels.
3. These parameters correspond to a minimum setup time of 1 ns and a minimum hold time of 1 ns.

Table 247. AC Specifications for RGMII 10/100 Mbps

Symbol	Parameter	Condition	Minimum	Typical (1)	Maximum	Unit
f	Clock frequency	100 Mbps		25		MHz
		10 Mbps		2.5		MHz
	Clock frequency stability		–50		50	ppm
t_c	Clock cycle time	100 Mbps	36	40	44	ns
		10 Mbps	360	400	440	ns
	Clock duty cycle	1.25 V	40	50	60	%
t_r	RGMII signal rise time	20% to 80% (2)			0.75	ns
t_f	RGMII signal fall time	80% to 20% (2)			0.75	ns
$t_{sk(T)}$	Data to clock output skew	1.25 V	–500	0	500	ps
$t_{sk(R)}$	Data to clock input skew	1.25 V	1			ns
$t_{su(T)}$	Data setup to clock in compensated mode	1.25 V	1.2	2.0		ns
$t_{h(T)}$	Data hold from clock in compensated mode	1.25 V				ns
$t_{sk(RC)}$	Data to clock input skew in compensated mode	1.25 V	–1		0.6	ns

1. Typical values are at 25°C.
2. Measured relative to worst-case DC output levels.

Figure 39. RGMII Test Circuit



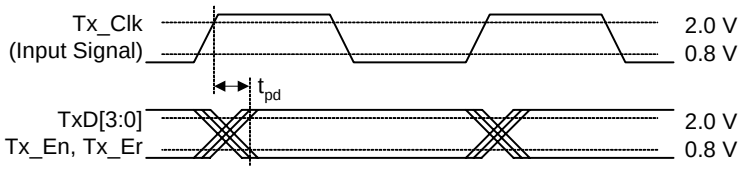
7.3.4 AC Specifications for MII (10/100 Mbps)

All AC specifications for the MII meet or exceed the requirements of IEEE Std 802.3-2002 (Clause 22.3-4).

7.3.4.1 MII Transmit

The propagation delay from a MII clock to a valid MII signal is defined as the length of time between when the clock exits the switching region and when the signal exits and remains out of the switching region. The following figure shows the MII transmit waveforms and required measurement points for the different signals.

Figure 40. MII Transmit Timing Diagram



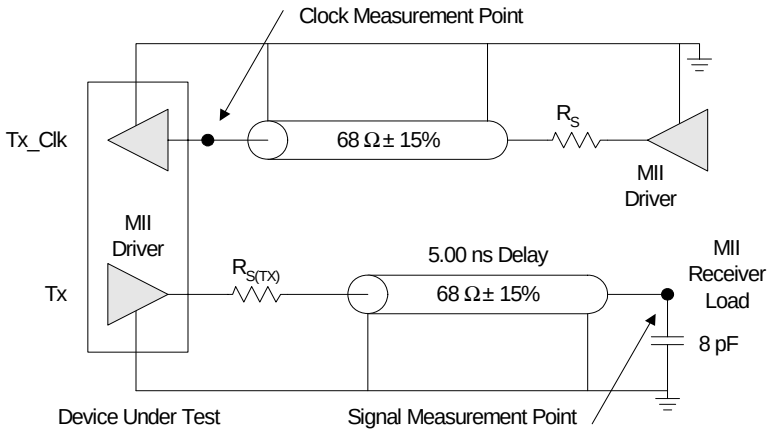
The following table contains the requirement or specifications for MII transmit signals at the pins of the SparX-G5e device.

Table 248. AC Specifications for MII Transmit

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f	Tx_Clk frequency	100 Mbps operation	25 – 100 ppm	25 + 100 ppm	MHz
		10 Mbps operation	2.5 – 100 ppm	2.5 + 100 ppm	MHz
	Tx_Clk duty cycle	1.4 V	35	65	%
t_{pd}	TxD, Tx_En, Tx_Er delay from Tx_Clk		0	15	ns

The TxD[3:0], Tx_En, and Tx_Er propagation delay, compared to the Tx_Clk, is measured in accordance with the following figure, but measured as the time difference between the clock measurement point and the signal measurement point. From this, the delay through the Tx transmission line (that is, 5.00 ns) is then subtracted.

Figure 41. MII Test Circuit



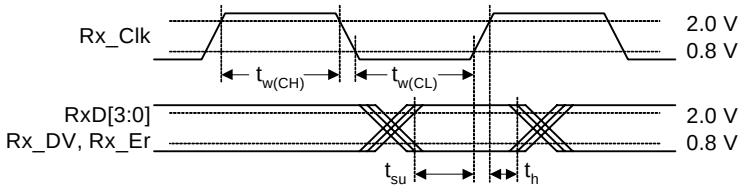
7.3.4.2 MII Receive

The setup time of an MII signal relative to the clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region.

The hold time of an MII signal relative to the clock edge is defined as the length of time between when the clock exits the switching region and when the signals enters the switching region.

The following figure shows the MII receive waveforms and required measurement points for the different signals.

Figure 42. MII Receive Timing Diagram



All signals applied to the MII input pins should fulfill the requirements in the following two tables, depending on the data speed.

Table 249. AC Specifications for MII Receive (100-Mbps Operation)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f	Rx_Clk frequency	Rx_DV asserted		25		MHz
	Rx_Clk duty cycle	Rx_DV asserted @ 1.4 V	35		65	%
$t_{w(CH)}$	Rx_Clk time high	Always	14		80	ns
$t_{w(CL)}$	Rx_Clk time low	Always	14		80	ns

Table 249. AC Specifications for MII Receive (100-Mbps Operation) *(continued)*

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{su}	RxD, Rx_DV, Rx_Er setup to Rx_Clk		10			ns
t_h	RxD, Rx_DV, Rx_Er hold to Rx_Clk		10			ns

Table 250. AC Specifications for MII Receive (10-Mbps Operation)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f	Rx_Clk frequency	Rx_DV asserted		2.5		MHz
	Rx_Clk duty cycle	Rx_DV asserted @ 1.4 V	35		65	%
$t_{w(CH)}$	Rx_Clk time high	Always	140		800	ns
$t_{w(CL)}$	Rx_Clk time low	Always	140		800	ns
t_{su}	RxD, Rx_DV, Rx_Er setup to Rx_Clk		10			ns
t_h	RxD, Rx_DV, Rx_Er hold to Rx_Clk		10			ns

Col and CRS signals are asynchronous to the clock and consequently do not have any setup and hold time requirements.

7.3.5 AC Specifications for GMII (1000 Mbps)

All AC specifications for the GMII have been designed to meet or exceed the requirements of IEEE Std 802.3-2002 (Clause 35.4.2).

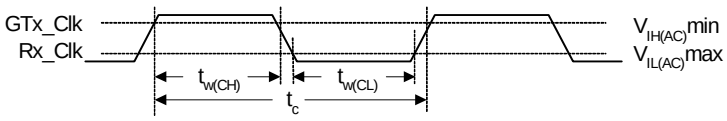
All GMII AC timing requirements are specified relative to the $V_{IL(AC)}$max and $V_{IH(AC)}$min threshold voltages specified in the following table.

Table 251. AC Voltage Threshold Levels for GMII

Symbol	Parameter	Minimum	Maximum	Unit
$V_{IL(AC)}$	Input low voltage AC		0.70	V
$V_{IH(AC)}$	Input high voltage AC	1.90		V

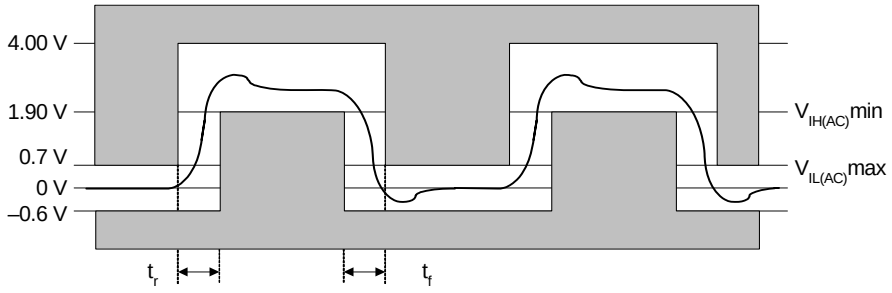
The following figure shows the definitions for the GMII clocks (GTx_Clk and Rx_Clk) parameters t_c, $t_{w(CH)}$, and $t_{w(CL)}$.

Figure 43. GTx_Clk and Rx_Clk Timing Parameters at Receiver Input



The following figure defines the clocks' rise time and fall time parameters (t_r and t_f) and other transient performance specifications. The figure defines a template with which all GMII signals must comply at the input of a GMII receiver.

Figure 44. GMII Receiver Input Potential Template



Note As measured at the measurement point in Figure 46.

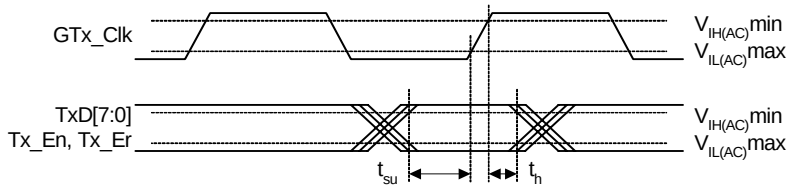
The setup time of an GMII signal relative to the clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region.

The hold time of an GMII signal relative to the clock edge is defined as the length of time between when the clock exits the switching region and when the signals enters the switching region.

7.3.5.1 GMII Transmit

The following figure shows the GMII transmit waveforms and required measurement points.

Figure 45. GMII Transmit Timing Diagram



All GMII transmit signals comply with the template shown in Figure 44, when measured using the test circuit in Figure 46. All the timing measurements (except setup and hold time) use the test circuit in Figure 46. The setup and hold time measurements use the test circuit in Figure 47.

Table 252. AC Specifications for GMII Transmit

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f	GTx_Clk frequency		125 – 100 ppm	125 + 100 ppm	MHz
t_c	GTx_Clk cycle time		7.50	8.50	ns
$t_{w(CH)}$	GTx_Clk time high		2.50		ns
$t_{w(CL)}$	GTx_Clk time low		2.50		ns
t_r	GTx_Clk rise time	$V_{IL(AC)}$max to $V_{IH(AC)}$min		1.00	ns

Table 252. AC Specifications for GMII Transmit *(continued)*

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_f	GTx_Clk fall time	$V_{IH(AC)}$min to $V_{IL(AC)}$max		1.00	ns
	Slew rate of GTx_Clk (rising)	$V_{IL(AC)}$max to $V_{IH(AC)}$min	0.6		V/ns
	Slew rate of GTx_Clk (falling)	$V_{IH(AC)}$min to $V_{IL(AC)}$max	0.6		V/ns
t_{su}	TxD, Tx_En, Tx_Er setup to GTx_Clk		2.50		ns
t_h	TxD, Tx_En, Tx_Er hold from GTx_Clk		0.50		ns

Figure 46. GMII Point-to-Point Test Circuit

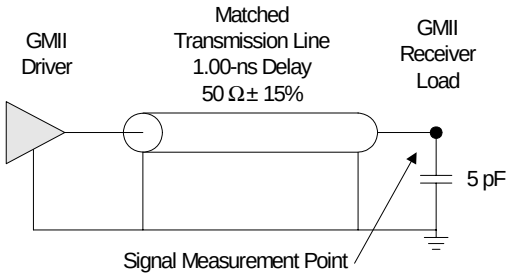
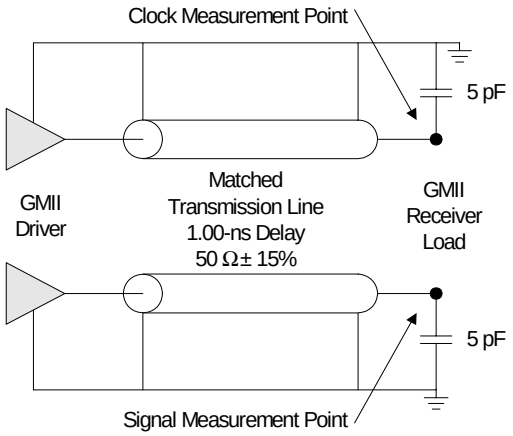


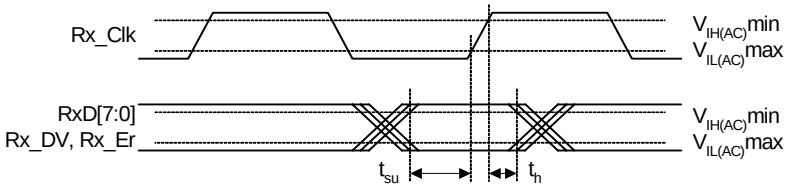
Figure 47. GMII Setup and Hold Time Test Circuit



7.3.5.2 GMII Receive

The following figure shows the GMII receive waveforms and required measurement points.

Figure 48. GMII Receive Timing Diagram



All GMII receive signals applied to the SparX-G5e device must comply with the template shown in Figure 44, page 230 according to the GMII standard. All signals applied to the GMII receiver inputs should comply with the requirements in the following table at the pins of the SparX-G5e device.

Table 253. AC Specifications for GMII Receive

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_c	Rx_Clk cycle time		7.50		ns
$t_{w(CH)}$	Rx_Clk time high		2.50		ns
$t_{w(CL)}$	Rx_Clk time low		2.50		ns
t_r	Rx_Clk rise time	$V_{IL(AC)}$max to $V_{IH(AC)}$min		1.00	ns
t_f	Rx_Clk fall time	$V_{IH(AC)}$min to $V_{IL(AC)}$max		1.00	ns
	Slew rate of Rx_Clk (rising)	$V_{IL(AC)}$max to $V_{IH(AC)}$min	0.6		V/ns
	Slew rate of Rx_Clk (falling)	$V_{IH(AC)}$min to $V_{IL(AC)}$max	0.6		V/ns
t_{su}	RxD, Rx_DV, Rx_Er setup to Rx_Clk		2.00		ns
t_h	RxD, Rx_DV, Rx_Er hold to Rx_Clk		0.00		ns

7.3.6 AC Specifications for MII Management

All AC specifications for the MII Management interface have been designed to meet or exceed the requirements of IEEE Std 802.3-2002 (Clause 22.2-4).

The supply voltage for the MII Management interface follows the supply voltage of the tri-speed ports (VDD_IOMAC). The timing reference levels are specified as follows:

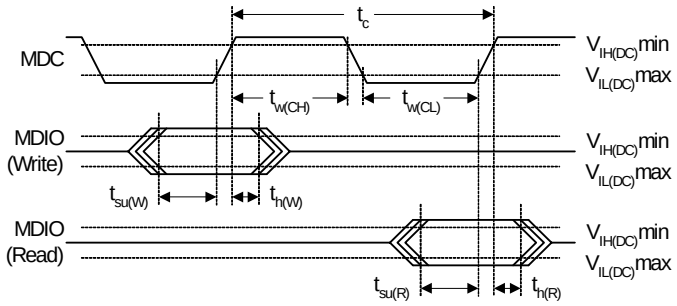
MII/GMII: 0.8 V and 2.0 V

RGMII: 0.7 V and 1.7 V

Additionally, the MDC signal must be monotonically in the switching region between $V_{IL(DC)}$max and $V_{IH(DC)}$min.

The following figure shows the MII management waveforms and required measurement points for the signals.

Figure 49. MII Management Timing Diagram



The setup time of MDIO relative to the rising edge of MDC is defined as the length of time between when the MDIO exits and remains out of the switching region and when MDC enters the switching region. The hold time of MDIO relative to the rising edge of MDC is defined as the length of time between when MDC exits the switching region and when MDIO enters the switching region.

All MII management transmit signals comply with the specifications in the following table. The MDIO signal requirements are requested at the pin of the SparX-G5e device.

Table 254. AC Specifications for MII Management

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f	MDC frequency		1.66	20	MHz
t_c	MDC cycle time		50		ns
$t_{w(CH)}$	MDC time high	C_L = 50 pF	20		ns
$t_{w(CL)}$	MDC time low	C_L = 50 pF	20		ns
$t_{su(W)}$	MDIO setup to MDC on write	C_L = 50 pF	15		ns
$t_{h(W)}$	MDIO hold from MDC on write	C_L = 50 pF	15		ns
$t_{su(R)}$	MDIO setup to MDC on read	C_L = 50 pF on MDC	15		ns
$t_{h(R)}$	MDIO hold from MDC on read		0		ns

The rate of MDC for both controllers can be configured in the range from 1.2 MHz to 78 MHz, but is only guaranteed to work over the full device temperature range up to 20 MHz.

7.3.7 AC Specifications for SI (Serial CPU Interface)

All SI AC timing requirements are specified relative to respectively the input low and high threshold level.

The SI timing parameters and required measurement points are defined in the following two figures.

Figure 50. SI Input Data Timing Diagram

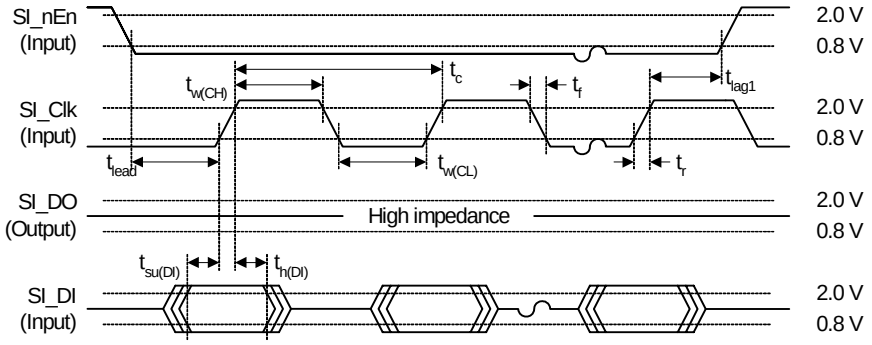
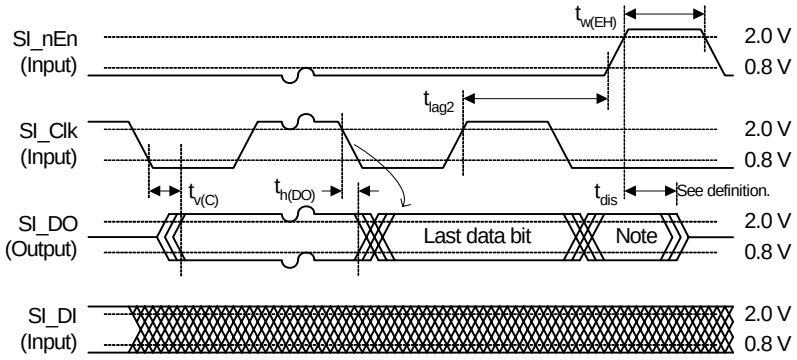


Figure 51. SI Output Data Timing Diagram



Note: Not defined, but this is normally the first bit from the next address.

All SI signals comply with the specifications in the following table, and the SI receive signal requirements are requested at the pins of the SparX-G5e device.

Table 255. AC Specifications for SI

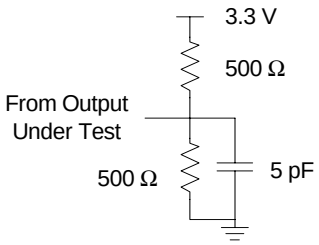
Symbol	Parameter	Condition	Minimum	Maximum	Unit
f	Clock frequency			25 (1)	MHz
t_c	Clock cycle time		40 (1)		ns
$t_{w(CH)}$	Clock time high		16		ns
$t_{w(CL)}$	Clock time low		16		ns
t_r, t_f	Clock rise time and fall time	Between V_{IL} and V_{IH}		10	ns
$t_{su(DI)}$	DI setup to clock		4		ns

Table 255. AC Specifications for SI *(continued)*

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{h(DI)}$	DI hold from clock		4		ns
t_{lead}	Enable active before first clock		10		ns
t_{lag1}	Enable inactive after clock (input cycle) (2)		25		ns
t_{lag2}	Enable inactive after clock (output cycle)		See note 3.		ns
$t_{w(EH)}$	Enable inactive width		20		ns
$t_{v(C)}$	DO valid after clock	C_L = 30 pF		12	ns
$t_{h(DO)}$	DO hold from clock	C_L = 0 pF	0		ns
t_{dis} 4	DO disable time	See Figure 52		15 (4)	ns

1. The SI clock frequency may be up to 25 MHz, but if it exceeds 1.25 MHz, dummy bytes must be inserted.
2. t_{lag1} is only defined for write operations to the SparX-G5e device, not read operations.
3. The last rising edge on the clock is necessary for the master to be able to read in the data. The lag time depends on the necessary hold time on the master data input.
4. The pin begins to float when a 300-mV change from the loaded V_{OH}/V_{OL} level occurs.

Figure 52. Test Circuit for SI_DO Disable Test

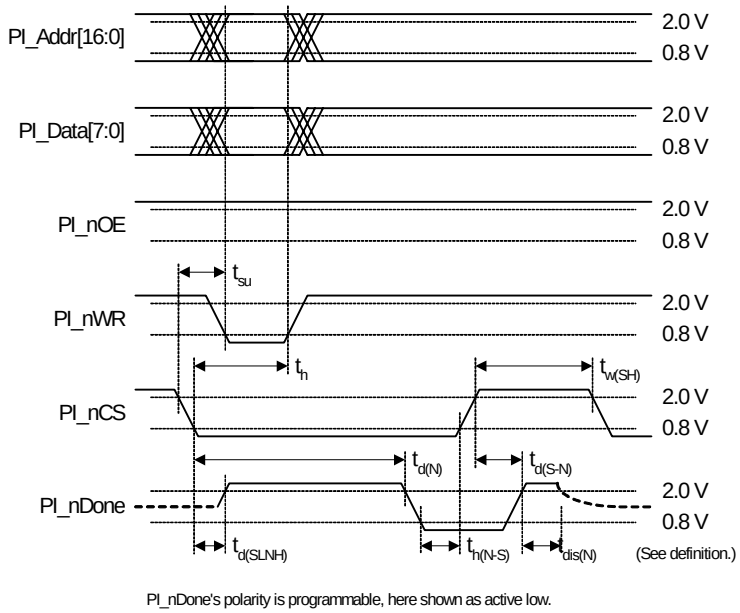


7.3.8 AC Specifications for PI (Parallel CPU Interface)

The AC timing provided in this section applies when the parallel interface is enabled.

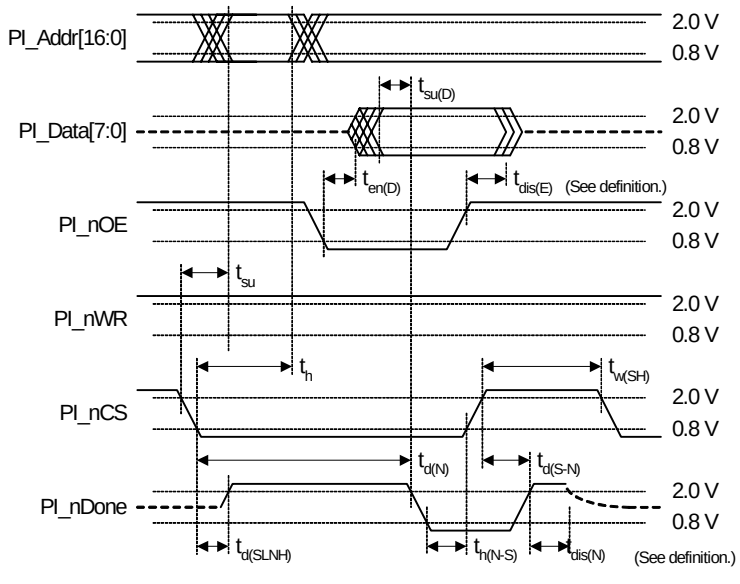
All PI AC timing requirements are specified relative to the input low and high threshold level. The PI timing parameters and required measurement points are defined in the following two figures.

Figure 53. PI Write Cycle (Input to the SparX-G5e Device)



PI_nDone's polarity is programmable, here shown as active low.

Figure 54. PI Read Cycle Timing Diagrams



PI_nDone's polarity is programmable, here shown as active low.

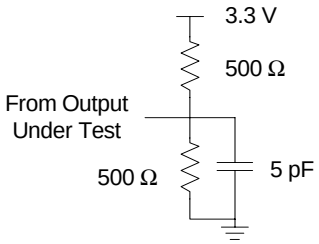
All PI signals comply with the specification in the following table, and the PI receive signal requirements are requested at the pins of the SparX-G5e device.

Table 256. AC Specifications for PI

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{su}	Addr, Data, nWR setup to nCS falling	Data only on write	–4 (1)		ns
t_h	Addr, Data, nWR hold from nCS low	Data only on write	25 (1)		ns
$t_{d(SLNH)}$	Delay from nCS low to nDone rising (2)	C_L = 30pF		10	ns
$t_{d(N)}$	Delay from nCS low to nDone falling (2)	C_L = 30pF		55 (1, 3)	ns
$t_{h(N-S)}$	nCS hold from nDone falling (2)		0		ns
$t_{d(S-N)}$	Delay from nCS high to nDone high (2)	C_L = 30pF		10	ns
$t_{dis(N)}$	nDone disable time from nDone pulled inactive (2, 4)	See Figure 55		12	ns
$t_{w(SH)}$	Width of nCS high		10		ns
$t_{en(D)}$	nOE and nCS low to data enabled(1, 5)	C_L = 30pF		15 (5)	ns
$t_{su(D)}$	Data setup to nDone falling on read (2)	C_L = 30pF	4		ns
$t_{dis(E)}$	Data disable time from either nCS or nOE high(4, 5)	See Figure 55		15	ns

1. An initial delay can be added before input data/conditions are sampled. It can be added in steps of 12.8 ns from 0 ns to 192 ns. The default is 192 ns to ensure operation with slow CPUs, but it is recommended to change this value. Timing in this table is shown with 0 ns delay.
2. nDone polarity is programmable, here it is illustrated as active low.
3. When using extended bus cycles, the response time can be up to 250 ns.
4. The pin begins to float when a 300-mV change from the loaded V_{OH}/V_{OL} level occurs.
5. Internal data output enable requires both nOE and nCS active. A time of 15 ns is only valid if PI_WAIT in the CPUCTRL register is set to 0x00 (for more information, see Table 80, page 153). If set to a value other than 0x00, the value shown here for $t_{en(D)}$ changes.

Figure 55. Test Circuit for Signal Disable Test



A reset of the interrupt status signal (PI_IRQ) caused by a read or write occurs simultaneously with the falling edge of PI_nDone, as shown in the following two figures.

Figure 56. PI Interrupt Write Cycle

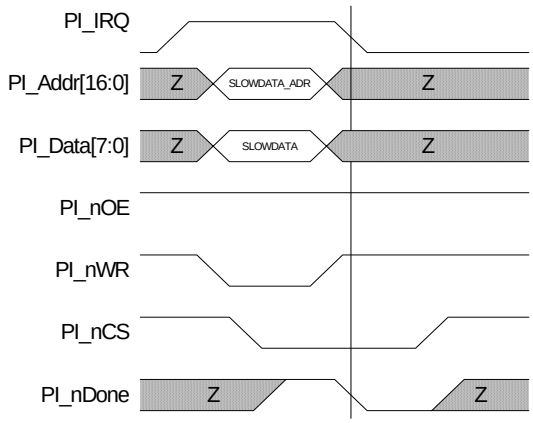
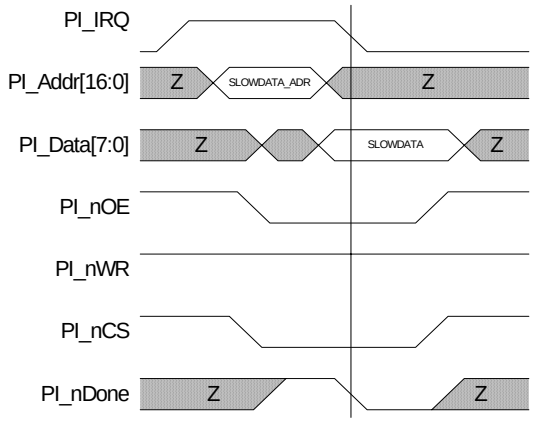


Figure 57. PI Interrupt Read Cycle



7.3.9 V-Core CPU External Memory Interface

The figures and tables in this section refer to the V-Core CPU's external RAM/ROM interface. This only applies when the V-Core CPU has access to the parallel interface, that is, when the ICPU_PI_En strapping pin is strapped high.

For more information about the pin mapping, see "Pin Name Mapping," page 103.

7.3.9.1 V-Core CPU RAM Read

The V-Core CPU timing parameters and required measurement points for a RAM read access are defined in the following figure. All V-Core CPU signals comply with the specification in Table 257, page 240.

Figure 58. V-Core CPU RAM Read

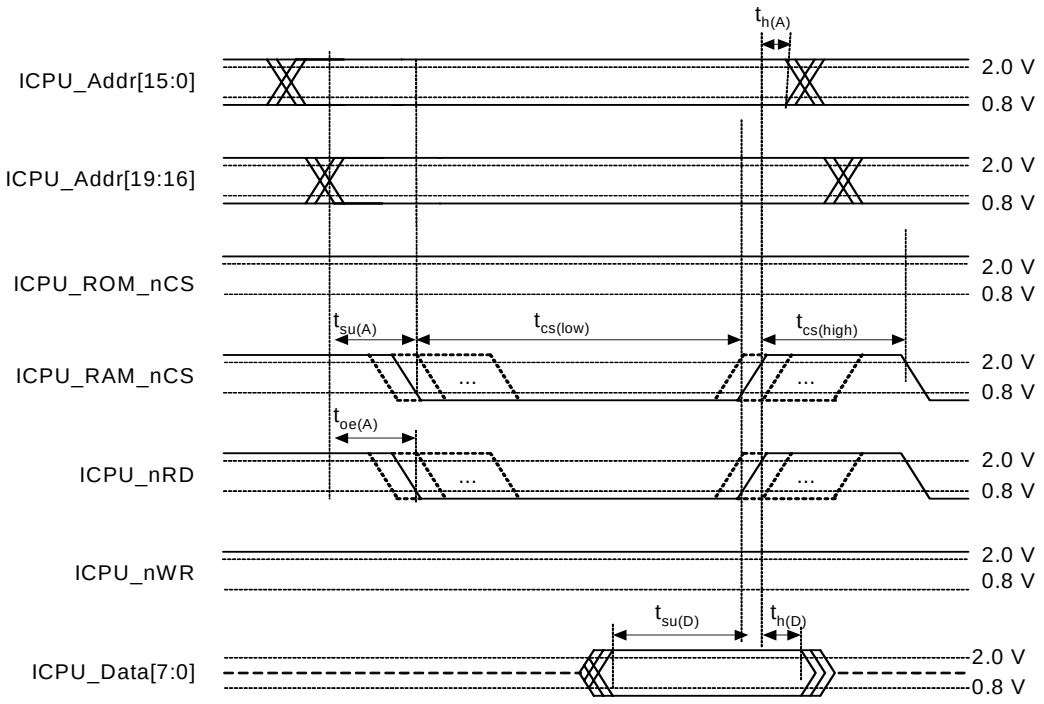


Table 257. V-Core CPU RAM Read Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{su(A)}$	Address setup to RAM Chip Select	C_L = 30 pF	2 (1)		ns
$t_{h(A)}$	Address hold from RAM Chip Select	C_L = 30 pF	194 (2)		ns
$t_{cs(low)}$	Chip Select low	C_L = 30 pF	815 (3)	823 (3)	ns
$t_{cs(high)}$	Chip Select high before new access	C_L = 30 pF	205 (4)		ns
$t_{oe(A)}$	Address setup to RAM Read/OE	C_L = 30 pF	2 (5)		ns
$t_{su(D)}$	Data setup to Chip Select high	C_L = 30 pF	33 (6)		ns
$t_{h(D)}$	Data hold from Chip Select high	C_L = 30 pF	0		ns

1. RAM Chip Select (ICPU_RAM_nCS) can be delayed from 0 to 44.8 ns in steps of 6.4 ns. The default is 6.4 ns. This is controlled through the CHIP::SYSTEM::ICPU_RAM_CFG register's CHIP_SEL_READ_DELAY field. Address setup to RAM Chip Select depends on the delay. If the RAM Chip Select delay is 0 ns, the maximum setup time is –4.4 ns. If the RAM Chip Select delay is 44.8 ns, the minimum setup time is 40.4 ns.
2. Addresses are held one CPU clock minus the RAM Chip Select delay and minus 4 ns.
   The default CPU clock is 156.25 MHz divided by 32, giving 4.9 MHz (205 ns). The default delay is 1 ns, which gives 205 – 6.4 – 4 = 194 ns. Notice that the Address hold can be negative if the CPU clock is fast and the delay is big.
3. The RAM Chip Select (ICPU_RAM_nCS) low time is determined by two parameters. The first parameter is a division of the system clock (156.25 MHz) to generate the CPU clock. This is controlled through the CHIP::SYSTEM::ICPU_CTRL register's CLK_DIV field. The division can be from 2 to 32 times, giving a CPU clock from approximately 4.9 MHz to 78.1 MHz. The default is 32 times. The second parameter is the RAM Chip Select low time, which can be set through the SFR::CKCON::MD register to 2, 4, 8, 12, …, or 28 8051 clock cycles; the default is four. A clock divisor of 7 yields a frequency of approximately 22.3 MHz and with the MD parameter set to 2 clock cycles, the RAM Chip Select low time is at least 89 ns. If the Chip Select delay is 6.4 ns, a 55 ns RAM can be used (Chip Select to Data Out).
4. The Chip Select high is minimum one CPU clock; the default 4.9 MHz gives 205 ns.
5. The Read signal (ICPU_nRD) can also be delayed from 0 to 44.8 ns, in steps of 6.4 ns. The default is 6.4 ns. This is controlled through the CHIP::SYSTEM::ICPU_RAM_CFG register's READ_DELAY field. The length of Read low is the same as for RAM Chip Select (see note 3 above).
6. The setup time for Data to RAM Chip Select depends on the delay for the RAM Chip Select. For the default delay of 6.4 ns, the setup time is 33 ns. If the delay is 0 ns, the setup time is 27 ns; with a delay of 44.8 ns, the setup time is minimum 72 ns.

7.3.9.2 V-Core CPU ROM/Flash Read

The V-Core CPU timing parameters and required measurement points for a ROM/Flash read access are defined in the following figure. All V-Core CPU signals for the ROM/Flash read access comply with the specification in Table 258, page 242.

Figure 59. V-Core CPU ROM/Flash Read

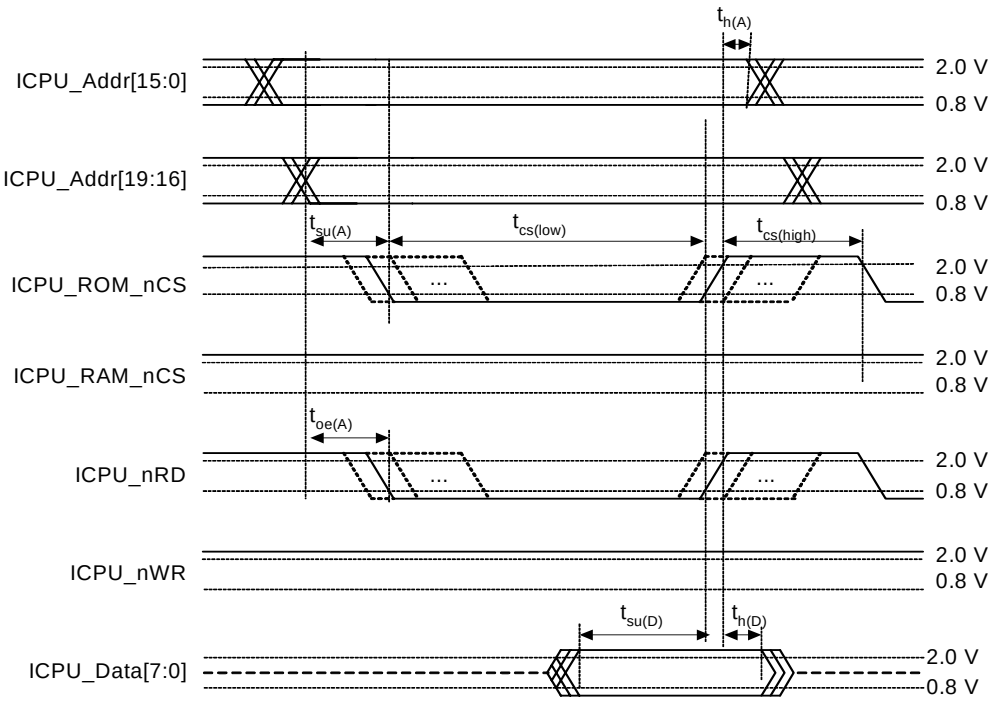


Table 258. V-Core CPU ROM/Flash Read Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{su(A)}$	Address setup to ROM Chip Select	C_L = 30 pF	2 (1)		ns
$t_{h(A)}$	Address hold from ROM Chip Select	C_L = 30 pF	194 (2)		ns
$t_{cs(low)}$	Chip Select low	C_L = 30 pF	406 (3)	414 (3)	ns
$t_{cs(high)}$	Chip Select high before new access	C_L = 30 pF	205 (4)		ns
$t_{oe(A)}$	Address setup to ROM Read/OE	C_L = 30 pF	2 (5)		ns
$t_{su(D)}$	Data setup to Chip Select high	C_L = 30 pF	33 (6)		ns
$t_{h(D)}$	Data hold from Chip Select high	C_L = 30 pF	0		ns

1. ROM Chip Select (ICPU_ROM_nCS) can be delayed from 0 ns to 44.8 ns in steps of 6.4 ns. The default is 6.4 ns. This is controlled through the CHIP::SYSTEM::ICPU_ROM_CFG register's CHIP_SEL_READ_DELAY field. Address setup to ROM Chip Select depends on the delay. If the ROM Chip Select delay is 0 ns, the worst-case setup time is –4.4 ns. If the ROM Chip Select delay is 44.8 ns, the minimum setup time is 40.4 ns.
2. Addresses are held one CPU clock minus the ROM Chip Select delay and minus 4 ns.
   The default CPU clock is 156.25 MHz divided by 32, giving 4.9 MHz (205 ns). The default delay is 1 ns, which gives 205 – 6.4 – 4 = 194 ns. Notice that the Address hold can be negative if the CPU clock is fast and the delay is big.
3. As opposed to the other types of accesses, the ROM Chip Select (ICPU_ROM_nCS) low time is determined by only one parameter: the V-Core CPU's current clock frequency, which may be changed using the CHIP::SYSTEM::ICPU_CTRL register's CLK_DIV field. The frequency can range from approximately 4.9 MHz to 78.1 MHz, with the default being 4.9 MHz. The value of the SFR::CKCON::MD bits have no effect on the number of clock cycles that ROM Chip Select is low for reads. It is always two 8051 clock cycles.
4. The Chip Select high is minimum one CPU clock; the default 4.9 MHz gives 205 ns.
5. The Read signal (ICPU_nRD) can also be delayed from 0 ns to 44.8 ns, in steps of 6.4 ns. The default is 6.4 ns, but can be modified using the CHIP::SYSTEM::ICPU_CTRL_ROM_CFG register's READ_DELAY field. The length of Read low is the same as for ROM Chip Select. See note 3 above.
6. The setup time for Data to ROM Chip Select depends on the delay for the ROM Chip Select. By default, that is, with a delay of 6.4 ns, the setup time is 33 ns. If the delay is 0 ns, the setup time is 27 ns; with a delay of 44.8 ns, the setup time is 72 ns.

7.3.9.3 V-Core CPU RAM Write

The V-Core CPU timing parameters and required measurement points for a RAM write access are defined in the following figure. All V-Core CPU signals for the RAM write access comply with the specification in Table 259, page 244.

Figure 60. V-Core CPU RAM Write

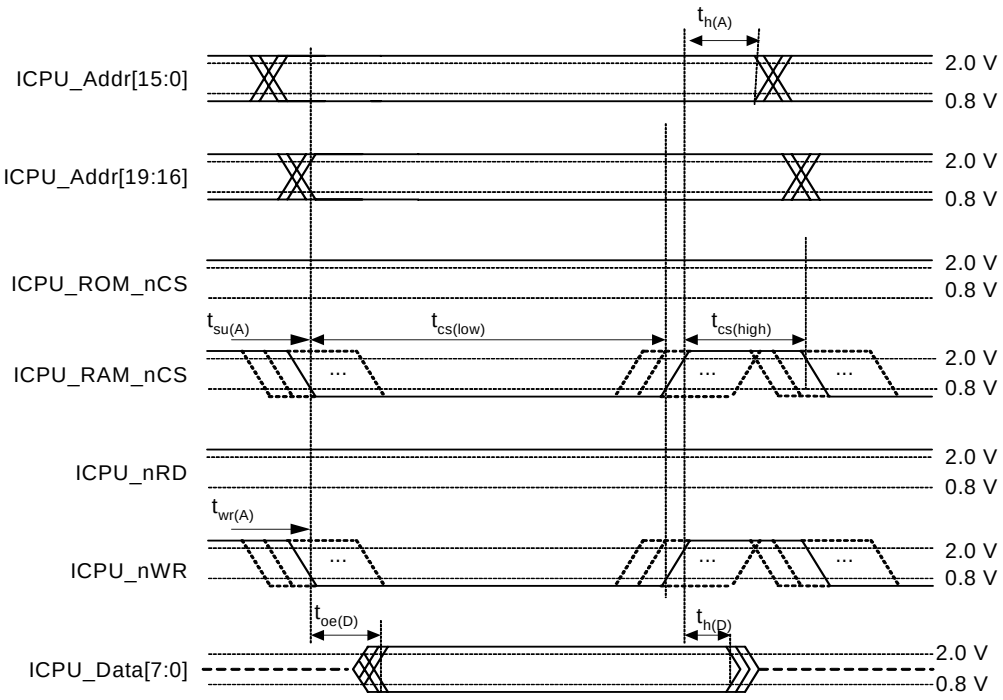


Table 259. V-Core CPU RAM Write Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{su(A)}$	Address setup to RAM Chip Select	C_L = 30 pF	8 (1)		ns
$t_{h(A)}$	Address hold from RAM Chip Select	C_L = 30 pF	194 (2)		ns
$t_{cs(low)}$	Chip Select low	C_L = 30 pF	815 (3)	823 (3)	ns
$t_{cs(high)}$	Chip Select high before new access	C_L = 30 pF	205 (4)		ns
$t_{wr(A)}$	Address setup to RAM Write	C_L = 30 pF	8 (5)		ns
$t_{oe(D)}$	Data valid from Chip Select	C_L = 30 pF		–4 (6)	ns
$t_{h(D)}$	Data hold from Chip Select high	C_L = 30 pF	2 (7)		ns

1. RAM Chip Select (ICPU_RAM_nCS) can be delayed from 0 ns to 44.8 ns in steps of 6.4 ns. The default is 12.8 ns in a write access. This is controlled through the CHIP::SYSTEM::ICPU_RAM_CFG register's CHIP_SEL_WRITE_DELAY field. Address setup to RAM Chip Select depends on the delay. If the RAM Chip Select delay is 0 ns, the worst-case setup time is –4 ns. If the RAM Chip Select delay is 44.8 ns, the minimum setup time is 40.8 ns.
2. Addresses are held one CPU clock minus the RAM Chip Select delay and minus 4 ns.
   The default CPU clock is 156.25 MHz divided with 32, giving 4.9 MHz (205 ns). The default delay is 1 ns, which gives 205 – 6.4 – 4 = 194 ns. Notice that the Address hold can be negative if the CPU clock is fast and the delay is big.
3. The RAM Chip Select (ICPU_RAM_nCS) low time is determined by two parameters. The first parameter is the V-Core CPU's clock frequency, which is controlled through the CHIP::SYSTEM::ICPU_CTRL register's CLK_DIV field. The frequency can range from 4.9 MHz to 78.1 MHz with the default being 4.9 MHz. The second parameter is the value of the SFR::CKCON::MD bits, which determines the number of 8051 clock cycles the RAM Chip Select signal is low. The default is 4 clock cycles, but can be changed to 2, 4, 8, 12, …, or 28 clock cycles.
4. The Chip Select high is minimum one CPU clock cycle; the default 4.9 MHz gives 205 ns.
5. The Write signal (ICPU_nWR) can also be delayed from 0 ns to 44.8 ns, in steps of 6.4 ns. The default is 12.8 ns for write accesses, but can be changed through the CHIP::SYSTEM::ICPU_RAM_CFG register's WRITE_DELAY field. The length of Write low is the same as for RAM Chip Select (see note 3 above).
6. Data valid from RAM Chip Select low is maximum –4 ns. The time depends on the RAM Chip Select delay. If the delay is 0 ns, the valid time is 10 ns; with a delay of 44.8 ns, the data valid time from RAM Chip Select is –41 ns.
7. Data can be extended in the end from 0 ns to 44.8 ns, in steps of 6.4 ns. The default is 19.2 ns, but this can be modified through the CHIP::SYSTEM::ICPU_RAM_CFG register's WRITE_DATA_HOLD field. The default of 19.2 ns gives a hold time of 2 ns (RAM Chip Select delay default is 12.8 ns). If the RAM Chip Select is delayed, for example, 25.6 ns, the data has to be extended with 19.2 ns to maintain a hold of 2 ns. Set these parameters carefully, because they can be set such that one cycle may overlap the next.

7.3.9.4 V-Core CPU Flash Write

The V-Core CPU timing parameters and required measurement points for a Flash write access are defined in the following figure. All V-Core CPU signals for the Flash write access comply with the specification in Table 260, page 246.

Figure 61. V-Core CPU Flash Write

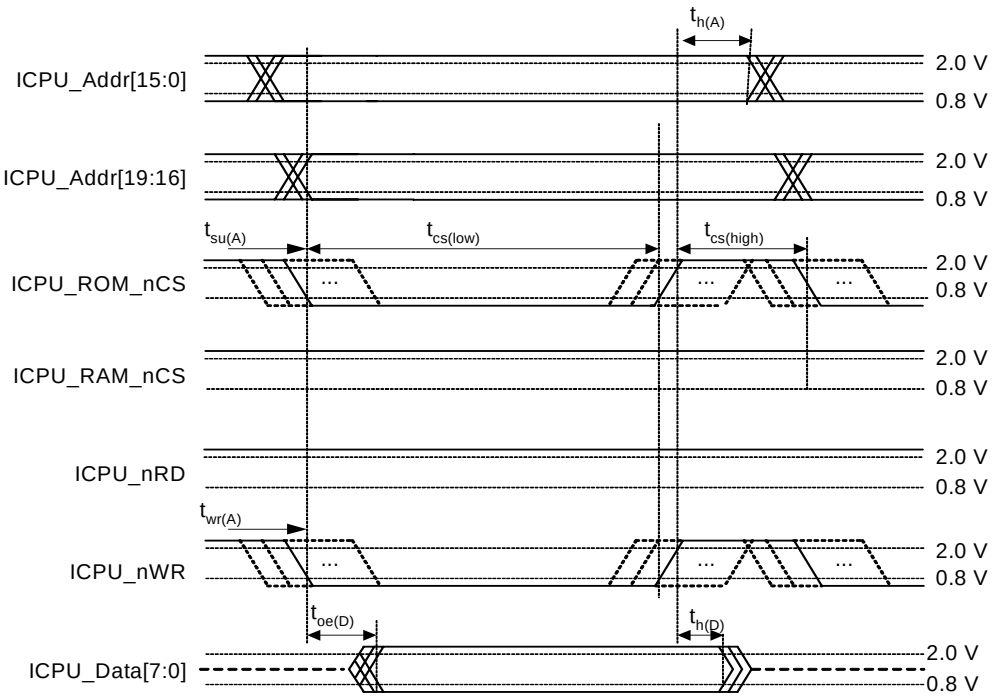


Table 260. V-Core CPU Flash Write Specifications

Symbol	Parameter	Condition	Minimum	Maximum	Unit
$t_{su(A)}$	Address setup to ROM Chip Select	C_L = 30 pF	8 (1)		ns
$t_{h(A)}$	Address hold from ROM Chip Select	C_L = 30 pF	194 (2)		ns
$t_{cs(low)}$	Chip Select low	C_L = 30 pF	815 (3)	823 (3)	ns
$t_{cs(high)}$	Chip Select high before new access	C_L = 30 pF	205 (4)		ns
$t_{wr(A)}$	Address setup to ROM Write	C_L = 30 pF	8 (5)		ns
$t_{oe(D)}$	Data valid from Chip Select	C_L = 30 pF		4 (6)	ns
$t_{h(D)}$	Data hold from Chip Select high	C_L = 30 pF	2 (7)		ns

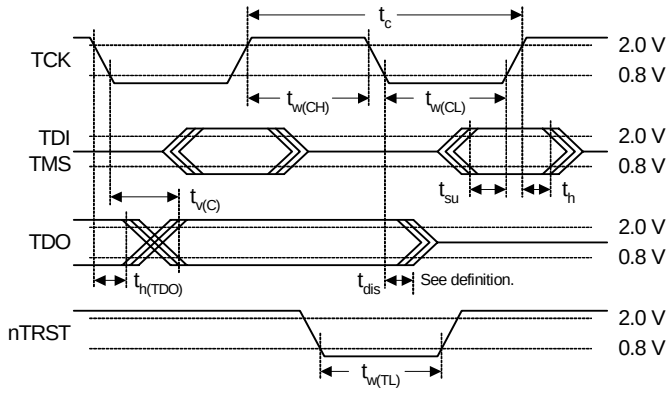
1. The ROM Chip Select (ICPU_ROM_nCS) can be delayed from 0 ns to 44.8 ns in steps of 6.4 ns. The default is 12.8 ns for write accesses. This is controlled through the CHIP::SYSTEM::ICPU_ROM_CFG register's CHIP_SEL_WRITE_DELAY field. Address setup to RAM Chip Select depends on the delay. If the ROM Chip Select delay is 0 ns, the setup time is worst-case –4 ns. If the ROM Chip Select delay is 44.8 ns, the minimum setup time is 40.8 ns.
2. Addresses are held one CPU clock minus the ROM Chip Select delay and minus 4 ns.
   The default CPU clock is 156.25 MHz divided by 32, giving 4.9 MHz (205 ns). The default delay is 1 ns, which gives 205 – 6.4 – 4 = 194 ns. Notice that the Address hold can be negative if the CPU clock is fast and the delay is big.
3. The ROM Chip Select (ICPU_ROM_nCS) low time is decided from two parameters. The first parameter is the V-Core CPU's clock frequency, which is controlled through the CHIP::SYSTEM::ICPU_CTRL register's CLK_DIV field. The frequency can range from approximately 4.9 MHz to 78.1 MHz, with default being 4.9 MHz. The second parameter is the value of the SFR::CKCON::MD bits, which determines the number of 8051 clock cycles the ROM Chip Select signal is low. The default is 4 clock cycles, but can be changed to 2, 4, 8, 12, …, or 28 clock cycles.
4. The Chip Select high is minimum one CPU clock cycle; the default 4.9 MHz gives 205 ns.
5. The Write signal (ICPU_nWR) can also be delayed from 0 ns to 44.8 ns, in steps of 6.4 ns. The default is 12.8 ns for write accesses, but this can be modified through the CHIP::SYSTEM::ICPU_ROM_CFG register's WRITE_DELAY field. The length of Write low is the same as for the ROM Chip Select (see note 3 above).
6. Data valid from ROM Chip Select low is maximum 4 ns. The time depends on the ROM Chip Select delay. If the delay is 0 ns, the valid time is 10 ns; with a delay of 44.8 ns, the data valid time from ROM Chip Select is –41 ns.
7. Data can be extended in the end from 0 ns to 44.8 ns, in steps of 6.4 ns. The default is 19.2 ns, but can be modified through the CHIP::SYSTEM::ICPU_ROM_CFG register's WRITE_DATA_HOLD field. The default of 19.2 ns gives a hold time of 2 ns (ROM Chip Select delay is 12.8 ns). If the ROM Chip Select is delayed, for example, 25.6 ns, the data has to be extended with 19.2 ns to maintain a hold of 2 ns. Set these parameters carefully, because they can be set such that one cycle may overlap the next.

7.3.10 AC Specifications for JTAG

All AC specifications for the JTAG interface have been designed to meet or exceed the requirements of IEEE Std 1149.1-2001.

The following figure shows the JTAG transmit and receive waveforms and required measurement points for the different signals.

Figure 62. JTAG Interface Timing Diagram



All JTAG signals comply with the specifications in the following table, and the JTAG receive signal requirements are requested at the pin of the SparX-G5e device.

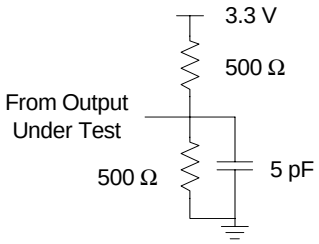
Table 261. AC Specifications for JTAG

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f	TCK frequency			10	MHz
t_c	TCK cycle time		100		ns
$t_{w(CH)}$	TCK time high		40		ns
$t_{w(CL)}$	TCK time low		40		ns
t_{su}	Setup to TCK rising		10		ns
t_h	Hold from TCK rising		10		ns
$t_{v(C)}$	TDO valid after TCK falling	C_L = 10 pF		28	ns
$t_{h(TDO)}$	TDO hold from TCK falling	C_L = 0 pF	0		ns
t_{dis}	TDO disable time (1)	See Figure 63		30 (1)	ns
$t_{w(TL)}$	nTRST time low		30		ns

1. The pin begins to float when a 300-mV change from the loaded V_{OH}/V_{OL} level occurs.

The JTAG_nTRST signal is asynchronous to the clock and consequently does not have a setup and hold time requirement.

Figure 63. Test Circuit for TDO Disable Test



7.3.11 Serial LED Output Timing

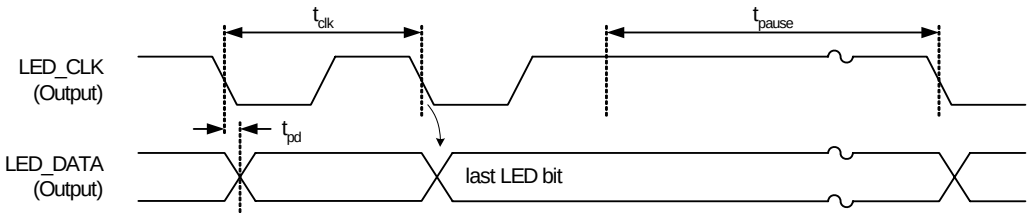
The specifications for Serial LED output are given in the following table and figure.

Table 262. Serial LED Output Timing

Symbol	Parameter	Minimum	Typical	Maximum	Unit
t_{clk}	LED_CLK period	1			µs
t_{pause}	The pause in between bursts of activity (1)		25		ms
t_{pd}	LED_DATA propagation delay	–15	0	15	ns

1. For more information about t_{pause}, see the functional timing in Figure 7, page 57.

Figure 64. Serial LED Output AC Timing Diagram



7.4 Operating Conditions

The following table shows the recommended operating conditions for the VSC7395 device.

Table 263. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD_A12}	Power supply voltage	1.14	1.20	1.26	V
V_{DD_A33}	Power supply voltage	3.13	3.30	3.45	V
V_{DD}	Core power supply voltage	1.14	1.20	1.26	V
V_{DD_IOCPU}	I/O power supply voltage	3.13	3.30	3.45	V
V_{DD_IOMAC}	3.3 V power supply voltage, MII and GMII mode	3.13	3.30	3.45	V
	2.5 V power supply voltage, RGMII mode	2.37	2.50	2.63	V
f	RefClk frequency, ±100 ppm (1)		25 / 125		MHz
T	VSC7395 operating temperature (2)	0		100	°C
T	VSC7395-03 operating temperature (2)	–40		100	°C

1. Except for RGMII mode, which is ±50 ppm.
2. Lower limit of specification is ambient temperature, and upper limit is case temperature.

7.5 Stress Ratings

This section contains the stress ratings for the VSC7395 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 264. Stress Ratings

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD_A12}	Power supply voltage	–0.5	1.4	V
V_{DD_A33}	Power supply voltage	–0.5	4.0	V
V_{DD}	Core power supply voltage	–0.5	1.4	V
V_{DD_IOCPU}	I/O power supply voltage	–0.5	4.0	V
V_{DD_IOMAC}	Power supply voltage	–0.5	4.0	V
V_{IN}	DC input voltage	–0.5	V_{DD_IOxxx} + 0.5 V	V
T_S	Storage temperature	–65	150	°C
V_{ESD_HBM}	Electrostatic discharge voltage, human body model	See note (1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

7.6 Power Sequencing

The nReset input should be held low until all power supply voltages have reached their recommended operating condition values.

8 Pin Descriptions

Many of the signal names used in the SparX-G5e are prefixed by the name of the interface to which they correspond to make it easier to distinguish the various signals from each other and to help relate a signal to the interface. Additionally, an active low signal is denoted with a lower case “n” as a prefix on the signal name (not interface name); for example PI_nOE.

Differential signals use a P or N suffix to distinguish their positive and negative parts; for example, P1_D2N and P1_D2P.

The abbreviations listed in the following table are used in this section to define the pin types used on the SparX-G5e device.

Table 265. Pin Type Definitions

Pin Type	Definition	Description
I	Digital input	Standard digital input signal. No internal pull-up or pull-down.
O	Digital output	Output only.
O_{ZC}	Impedance controlled output	Controlled 50-Ω integrated (on-chip) source series terminated, digital output signal. Used primarily for timing-sensitive MAC interface and 125-MHz clock output pins, in addition to IPD/ high-speed manufacturing test mode pins.
I/O	Bidirectional	
OZ	3-state output	
A	Analog	
A_{DIFF}	Analog differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog bias	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network.
Power	Power	
GND	Ground	
INC	Internally not connected	The ball is not connected internally.
NC	No connection, do not connect	
3V	3.3 V tolerant	
5V	5 V tolerant	
PD	Pull-down	On-chip 100-kΩ pull-down resistor.
PU	Pull-up	On-chip 100-kΩ pull-up resistor.
TS	Built-in series termination	Optimized for driving 50-Ω transmissions, but not calibrated as O_{ZC}.

8.1 Pins by Function

This section provides descriptions of the pins used on the SparX-G5e device grouped according to their function. For more information about the pin names and pin numbers, see "Pins by Name," page 263 and "Pins by Number," page 267.

8.1.1 Power Supply and Ground Pins

Table 266. Power and Ground

Signal Name	Type	Description
VDD	Power	1.2 V core supply
VDD_A12	Power	1.2 V Analog supply
VDD_A33	Power	3.3 V Analog supply
VDD_IOMAC	Power	2.5 V or 3.3 V supply for the PHY interface
VDD_IOCPU	Power	3.3 V I/O supply
VSS	GND	Ground
VSS_IO	GND	Ground for VDD_IOMAC and VDD_IOCPU

8.1.2 Clock Circuits

Table 267. System Clock Interface

Signal Name	Type	Description
Osc_En	I, PU	Osc_En. This pin is sampled on the rising edge of nReset. If high (or left floating), then the on-chip oscillator circuit is enabled. If pulled low, the oscillator circuit is disabled and the device must be supplied with a 25-MHz or 125-MHz reference clock to the RefClk pin.
Clk125_En	I, PD	PLL mode select input. Clk125_En is sampled during the device power-up sequence or reset. When Clk125_En is pulled high, SparX-G5e expects a 125-MHz clock input as the reference clock. When left floating, a reference clock of 25 MHz is expected. For more information, see "Clock Configuration," page 276.
RefClk / Xtal1	I, 3V	Xtal1 – Crystal oscillator input. If enabled by floating Osc_En (or pulled high), a 25-MHz parallel resonant crystal should be connected across Xtal1 and Xtal2. In addition, 33-pF capacitors should be connected from Xtal1 and Xtal2, respectively, to GND. Clk125_En should be left floating (or pulled low) on reset. RefClk – Reference clock input. If enabled by pulling Osc_En low, the reference clock input can be sourced by the following clock sources: 25 MHz (Clk125_En is floating or pulled low). 125 MHz (Clk125_En is pulled high). For more information, see "Clock Configuration," page 276.

Table 267. System Clock Interface *(continued)*

Signal Name	Type	Description
Xtal2	I, PD	Crystal oscillator output. The parallel resonant crystal should be connected across Xtal1 and Xtal2. In addition, 33-pF capacitors should be connected from Xtal1 and Xtal2, respectively, to GND. If not using a crystal, this output pin can be left floating if driving Xtal1/RefClk with a reference clock.

8.1.3 Combined RGMII and GMII Interface

Table 268. Combined RGMII and GMII Interface

Signal Name	Type	Description
GMII_Col	I, PD	MII/GMII mode. Collision, active high. Indicates collision on the link. Collision is asserted by the attached PHY when a collision is sensed on the media. RGMII mode. Not used, can be left floating.
GMII_CRS	I, PD	MII/GMII mode. Carrier Sense, active high asynchronous input signal. Indicates traffic on the link. CRS is asserted by the attached PHY, when a nonidle condition is detected on the media. RGMII mode. Not used, can be left floating.
GMII_GTx_Clk	O_{ZC}	GMII mode. GMII Transmit Clock, 125 MHz. This clock is continuously driven from the MAC, and transmit data and control are synchronized to it. MII mode. Not used, leave unconnected. It can be disabled by writing to ADVPORTM register (Address 19h). It is low after a port reset. RGMII mode. Becomes Tx_Clk, same function as in GMII mode.
GMII_Rx_Clk	I	GMII/RGMII mode. Receive Clock, 125-MHz input. This clock is used to synchronize the receive data and control. MII mode. Receive clock, 2.5 MHz in 10-Mbps mode or 25 MHz in 100-Mbps mode. This clock is used to synchronize RxD, Rx_DV, and Rx_Er. If not used, pull high or low.
GMII_Rx_DV	I, PD	MII/GMII mode. Receive Data Valid. Active high. Rx_DV indicates that a receive frame is in progress and that the data present on the RxD input pins is valid. RGMII mode. Becomes RGMII_Rx_Ctrl.
GMII_Rx_Er	I, PD	MII/GMII mode. Receive Error Detected, active high. Indicates that an error has occurred during receiving. RGMII mode. Not used, can be left floating.
GMII_RxD0 GMII_RxD1 GMII_RxD2 GMII_RxD3 GMII_RxD4 GMII_RxD5 GMII_RxD6 GMII_RxD7	I, PD	GMII mode. Receive Data Inputs. Byte-wide receive data is sampled on these pins synchronous to Rx_Clk rising. RxD7 is the most significant bit. MII mode. Same as in GMII mode, except only RxD[3:0] are active. RxD[7:4] can be left floating. RGMII mode. Multiplexed receive data input. Only RxD[3:0] are active and becomes RD[3:0], RxD[7:4] can be left floating. Contains bit [3:0] on the rising edge of the Rx_Clk and bit [7:4] on the falling edge.
GMII_Tx_En	O_{ZC}	MII/GMII mode. Transmit Enable, active high. This output indicates that valid data is present on the TxD bus. RGMII mode. RGMII_Tx_Ctrl.

Table 268. Combined RGMII and GMII Interface *(continued)*

Signal Name	Type	Description
GMII_Tx_Er	O_{ZC}	MII/GMII mode. Transmit Error, active high. Used to signal a transmission error to the PHY. RGMII mode. Not used, can be left unconnected.
GMII_TxD0 GMII_TxD1 GMII_TxD2 GMII_TxD3 GMII_TxD4 GMII_TxD5 GMII_TxD6 GMII_TxD7	O_{ZC}	GMII mode. Transmit data outputs. Byte-wide transmit data synchronously to the GTx_Clk. TxD7 is the most significant bit. MII mode. Same as in GMII mode, except only TxD[3:0] are active, TxD[7:4] are low and can be left floating. RGMII mode. Multiplexed transmit data output. Only TxD[3:0] are active and become TD[3:0], TxD[7:4] are low and can be left floating. Contains bit [3:0] on the rising edge of the Tx_Clk and bit [7:4] on the falling edge.
MII__Tx_Clk	I	MII mode. MII Transmit Clock. This clock is used to synchronize the transmit data, enable, and error. In 100-Mbps mode, the input is a 25-MHz clock; in 10-Mbps mode, the input is a 2.5-MHz clock. All other modes. Not used, pull high or low.

8.1.4 MII and RGMII Signal Mappings

The signal mappings between MII, RGMII, and GMII follow the recommended signal mapping in IEEE Std 802.3-2002 (Clause 35.3).

The following table shows how the MII and RGMII signals are mapped onto the GMII signals.

Table 269. GMII Signal Mapping to Other Interfaces

Signal Name	Used in Mode		
	GMII	MII	RGMII
MII_ Tx_Clk		Tx_Clk	
GMII_GTx_Clk	GTx_Clk		Tx_Clk
GMII_Tx_Er	Tx_Er	Tx_Er	
GMII_Tx_En	Tx_En	Tx_En	Tx_Ctrl
GMII_TxD7	TxD7		
GMII_TxD6	TxD6		
GMII_TxD5	TxD5		
GMII_TxD4	TxD4		
GMII_TxD3	TxD3	TxD3	TD3
GMII_TxD2	TxD2	TxD2	TD2
GMII_TxD1	TxD1	TxD1	TD1
GMII_TxD0	TxD0	TxD0	TD0
GMII_Rx_Clk	Rx_Clk	Rx_Clk	Rx_Clk
GMII_Col	Col	Col	
GMII_Rx_Er	Rx_Er	Rx_Er	
GMII_Rx_DV	Rx_DV	Rx_DV	Rx_Ctrl
GMII_RxD7	RxD7		

Table 269. GMII Signal Mapping to Other Interfaces *(continued)*

Signal Name	Used in Mode		
	GMII	MII	RGMII
GMII_RxD6	RxD6		
GMII_RxD5	RxD5		
GMII_RxD4	RxD4		
GMII_RxD3	RxD3	RxD3	RD3
GMII_RxD2	RxD2	RxD2	RD2
GMII_RxD1	RxD1	RxD1	RD1
GMII_RxD0	RxD0	RxD0	RD0
GMII_CRS	CRS	CRS	

8.1.5 MII Management Interface

Table 270. MII Management Interface

Signal Name	Type	Description
MDIO	I/O, O_{ZC}, PU, 3V	Management data input/output. MDIO is a bidirectional signal between a PHY and SparX-G5e that transfers control and status information. Control information is driven by SparX-G5e synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by SparX-G5e.
MDC	O_{ZC}	Management data clock. MDC is sourced by the station management entity (SparX-G5e) to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal.

8.1.6 Parallel CPU Interface (PI)

The information provided in the following table only applies if the parallel interface is enabled. For more information about enabling the parallel interface, see "V-Core CPU," page 95 and Table 26, page 96.

Table 271. PI

Signal Name	Type	Description
PI_Addr0 PI_Addr1 PI_Addr2 PI_Addr3 PI_Addr4 PI_Addr5 PI_Addr6 PI_Addr7 PI_Addr8 PI_Addr9 PI_Addr10 PI_Addr11 PI_Addr12 PI_Addr13 PI_Addr14 PI_Addr15 PI_Addr16	I, PU, 3V	Least significant bit. Parallel CPU interface address bus. Selects the block, subblock, and address. For more information about the address space, see "Register Addressing," page 137. Most significant bit.
PI_Data0 PI_Data1 PI_Data2 PI_Data3 PI_Data4 PI_Data5 PI_Data6 PI_Data7	I/O, PU, 3V, TS	Least significant bit. Parallel CPU interface data bus. Driven by CPU at write, SparX-G5e at read. Most significant bit.
PI_IRQ_0 PI_IRQ_1	O, TS	A configurable interrupt signal for various events. The interrupt signal's polarity can be programmed. The Interrupt pin is not an open-drain output and should not be wire-ORed to other pins.
PI_nCS	I, PU, 3V	Start a CPU operation.
PI_nDone	OZ, 3V, TS, PU	Acknowledges an operation. Programmable polarity.
PI_nOE	I, PU, 3V	Enable drive of the data bus from SparX-G5e.
PI_nWR	I, PU, 3V	Selects read (1) or write (0).

8.1.7 V-Core CPU External Memory Interface

The information provided in the following table only applies if the V-Core CPU has access to the parallel interface, that is, when the ICPU_PI_En strapping pin is strapped high

Table 272. V-Core CPU External Memory Interface

Signal Name	Type	Description
ICPU_Addr0 ICPU_Addr1 ICPU_Addr2 ICPU_Addr3 ICPU_Addr4 ICPU_Addr5 ICPU_Addr6 ICPU_Addr7 ICPU_Addr8 ICPU_Addr9 ICPU_Addr10 ICPU_Addr11 ICPU_Addr12 ICPU_Addr13 ICPU_Addr14 ICPU_Addr15	O, TS	Least significant bit. V-Core CPU's address interface to external memories. Most significant bit.
ICPU_Addr16 ICPU_Addr17 ICPU_Addr18 ICPU_Addr19	O, TS	Least significant bit. Upper four bits of address, controlled through paging. Most significant bit.
ICPU_Data0 ICPU_Data1 ICPU_Data2 ICPU_Data3 ICPU_Data4 ICPU_Data5 ICPU_Data6 ICPU_Data7	I/O, PU, 3V, TS	Least significant bit. V-Core CPU's data interface to external memories. Driven by SparX-G5e on V-Core CPU-writes to external memories, driven by external memories on V-Core CPU-reads. Most significant bit.
ICPU_nWR	O, TS	Active low signal that selects write of external memory.
ICPU_nRD	O, TS	Active low signal that selects read of external memory.
ICPU_ROM_nCS	O, TS	Active low signal that selects external Flash/ROM.
ICPU_RAM_nCS	O, TS	Active low signal that selects external RAM.
ICPU_PI_En	I, PU	Strap high or leave floating to have the V-Core CPU access the parallel interface, or strap low to access the parallel interface from an external CPU.
ICPU_SI_Boot_En	I, PU	Pull high or leave floating to enable booting the V-Core CPU from an external EEPROM through the serial interface.

8.1.8 V-Core CPU GPIO and RS232 Interface

Table 273. V-Core CPU GPIO and RS232 Interface

Signal Name	Type	Description
ICPU_GPIO_0 ICPU_GPIO_1	I/O, PU, 3V, TS	Additional general-purpose I/Os only accessible from the V-Core CPU. These are only available if the ICPU_PI_En pin is strapped high.
ICPU_TxD	O, PU, TS	Serial data out of device.
ICPU_RxD	I, PU, 3V	Serial data in to device.

8.1.9 V-Core CPU Pin Mapping

The following table shows how the V-Core CPU pins are mapped to the PI. This is useful when locating pin numbers for the V-Core CPU pins, because the signal (pin) lists use the PI names. For more information about the pin lists, see "Pins by Name," page 263 and "Pins by Number," page 267.

Table 274. V-Core CPU Pin Mapping to the PI

V-Core CPU Signal Name	PI Signal Name	Comment
ICPU_GPIO_1	PI_IRQ_0	
ICPU_GPIO_0	PI_IRQ_1	
	PI_Addr16	Becomes output in V-Core CPU mode even though it is not used.
ICPU_Addr15	PI_Addr15	
ICPU_Addr14	PI_Addr14	
ICPU_Addr13	PI_Addr13	
ICPU_Addr12	PI_Addr12	
ICPU_Addr11	PI_Addr11	
ICPU_Addr10	PI_Addr10	
ICPU_Addr9	PI_Addr9	
ICPU_Addr8	PI_Addr8	
ICPU_Addr7	PI_Addr7	
ICPU_Addr6	PI_Addr6	
ICPU_Addr5	PI_Addr5	
ICPU_Addr4	PI_Addr4	
ICPU_Addr3	PI_Addr3	
ICPU_Addr2	PI_Addr2	
ICPU_Addr1	PI_Addr1	
ICPU_Addr0	PI_Addr0	
ICPU_Data7	PI_Data7	
ICPU_Data6	PI_Data6	
ICPU_Data5	PI_Data5	

Table 274. V-Core CPU Pin Mapping to the PI *(continued)*

V-Core CPU Signal Name	PI Signal Name	Comment
ICPU_Data4	PI_Data4	
ICPU_Data3	PI_Data3	
ICPU_Data2	PI_Data2	
ICPU_Data1	PI_Data1	
ICPU_Data0	PI_Data0	
ICPU_nWR	PI_nWR	
ICPU_nRD	PI_nOE	
ICPU_RAM_nCS	PI_nDone	
ICPU_ROM_nCS	PI_nCS	
ICPU_PI_En		
ICPU_SI_Boot_En		
ICPU_TxD		
ICPU_RxD		

8.1.10 Serial CPU Interface (SI)

The serial CPU interface can be used either as a serial slave interface used by an external CPU to access the SparX-G5e device or as a serial boot interface for the built-in CPU.

Table 275. SI

Signal Name	Type	Description
SI_nEn	I/O, PU, 3V, TS	0 = Enable SI slave interface. 1 = Disable SI slave interface. Output driven while booting from EEPROM (when ICPU_SI_Boot_En is pulled high or left floating). Released when booting is completed.
SI_Clk	I/O, PU, 3V, TS	Serial interface clock. Serial interface enabled. Clock signal from master. Serial interface disabled. If internal CPU is used and booting from EEPROM (ICPU_SI_Boot_En pulled high or left floating), this is the clock for the EEPROM.
SI_DI	I, PU, 3V	Serial input data.
SI_DO	PU, OZ, 3V, TS	Serial output data.

8.1.11 Twisted Pair Interface

Table 276. Twisted Pair Interface

Signal Name	Type	Description
P0_D0P P1_D0P P2_D0P P3_D0P P4_D0P	A_{DIFF}	Tx/Rx Channel A Positive Signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 1. For more information, see Figure 6, page 50.
P0_D0N P1_D0N P2_D0N P3_D0N P4_D0N	A_{DIFF}	Tx/Rx Channel A Negative Signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the A data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 2. For more information, see Figure 6, page 50.
P0_D1P P1_D1P P2_D1P P3_D1P P4_D1P	A_{DIFF}	Tx/Rx Channel B Positive Signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 3. For more information, see Figure 6, page 50.
P0_D1N P1_D1N P2_D1N P3_D1N P4_D1N	A_{DIFF}	Tx/Rx Channel B Negative Signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the B data channel. In all three speeds, these pins generate the secondary side signal, normally connected to RJ-45 pin 6. For more information, see Figure 6, page 50.
P0_D2P P1_D2P P2_D2P P3_D2P P4_D2P	A_{DIFF}	Tx/Rx Channel C Positive Signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the C data channel. In 1000-Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 4 (pins not used in 10/100 Mbps modes).For more information, see Figure 6, page 50.
P0_D2N P1_D2N P2_D2N P3_D2N P4_D2N	A_{DIFF}	Tx/Rx Channel C Negative Signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the C data channel. In 1000-Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 5 (pins not used in 10/100 Mbps modes). For more information, see Figure 6, page 50.
P0_D3P P1_D3P P2_D3P P3_D3P P4_D3P	A_{DIFF}	Tx/Rx Channel D Positive Signal. Positive differential signal connected to the positive primary side of the transformer. This pin signal forms the positive signal of the D data channel. In 1000-Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 7 (pins not used in 10/100 Mbps modes). For more information, see Figure 6, page 50.
P0_D3N P1_D3N P2_D3N P3_D3N P4_D3N	A_{DIFF}	Tx/Rx Channel D Negative Signal. Negative differential signal connected to the negative primary side of the transformer. This pin signal forms the negative signal of the D data channel. In 1000-Mb mode, these pins generate the secondary side signal, normally connected to RJ-45 pin 8 (pins not used in 10/100 Mbps modes). For more information, see Figure 6, page 50.

8.1.12 Analog Bias

Table 277. Analog Bias

Signal Name	Type	Description
Ref_RExt_0	A_{BIAS}	Reference External Resistor. Bias pin connects to an external resistor to analog ground. For more information, see "Analog Bias Pins Configuration," page 278.
Ref_Filt_0	A_{BIAS}	Reference Filter. Filter internal reference to an external capacitor to analog ground. For more information, see "Analog Bias Pins Configuration," page 278.

8.1.13 JTAG Interface

Table 278. JTAG Interface

Signal Name	Type	Description
JTAG_nTRST	I, PU, 5V	JTAG test reset, active low. For normal operation JTAG_nTRST should be pulled low.
JTAG_TCK	I, PU, 5V	JTAG clock.
JTAG_TDI	I, PU, 5V	JTAG test data in.
JTAG_TDO	PU, OZ, 3V, TS	JTAG test data out.
JTAG_TMS	I, PU, 5V	JTAG test mode select.

8.1.14 General-Purpose I/Os

Table 279. GPIO Signals

Signal Name	Type	Description
GPIO_0 GPIO_1 GPIO_2 GPIO_3	I/O, PU, 3V, TS	General-purpose I/O.

8.1.15 LED Interface

Table 280. LED Interface

Signal Name	Type	Description
LED[4:0]_0 LED[4:0]_1 LED[4:0]_2 LED[4:0]_3	O, TS	Direct-Drive LED Outputs. After reset, these pins serve as the direct drive, low EMI, LED driver output pins that can indicate individual status per pin. All LEDs are active-low and are powered by the VDD_A33 power supply. For information about how LED0_[1:0] can be configured to output a serial data stream, see "Serial LED Output," page 57.

8.1.16 Miscellaneous

Table 281. Miscellaneous Signals

Signal Name	Type	Description
nReset	I, PU, 3V	Global chip reset, active low.
INC_1 INC_2	INC	Leave floating
ThermDA	A	Thermal diodes anode (p-junction).
ThermDC	A	Thermal diodes cathode (n-junction). Connected internally to VSS.
Test_Code0 Test_Code1 Test_Code2	I, PU	Leave floating.
Reserved_3	I, 3V, PU	Internal test. Pull high or leave floating.
Reserved_4	I, 3V, PU	Internal test. Pull high or leave floating.
Reserved_0 Reserved_1 Reserved_2 Reserved_5	NC	Leave floating.

8.2 Pins by Name

This section provides an alphabetic list of the VSC7395 pins.

Table 282. Pins by Name

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
Clk125_En	J20	ICPU_PI_En	AB21	MII_Tx_Clk	AA13
GMII_Col	Y16	ICPU_RxD	AB20	nReset	AB2
GMII_CRS	AB17	ICPU_SI_Boot_En	AA20	Osc_En	K3
GMII_GTx_Clk	AB13	ICPU_TxD	Y19	P0_D0N	A18
GMII_Rx_Clk	AA17	INC_1	D1	P0_D0P	B18
GMII_Rx_DV	AB18	INC_2	C1	P0_D1N	A19
GMII_Rx_Er	Y17	JTAG_nTRST	U2	P0_D1P	B19
GMII_RxD0	AA16	JTAG_TCK	U3	P0_D2N	A20
GMII_RxD1	AB16	JTAG_TDI	V2	P0_D2P	B20
GMII_RxD2	Y15	JTAG_TDO	U1	P0_D3N	A21
GMII_RxD3	AA15	JTAG_TMS	V1	P0_D3P	B21
GMII_RxD4	AB15	LED0_0	E20	P1_D0N	A14
GMII_RxD5	Y14	LED0_1	F22	P1_D0P	B14
GMII_RxD6	AA14	LED0_2	F21	P1_D1N	A15
GMII_RxD7	AB14	LED0_3	F20	P1_D1P	B15
GMII_Tx_En	Y13	LED1_0	G22	P1_D2N	A16
GMII_Tx_Er	Y12	LED1_1	G21	P1_D2P	B16
GMII_TxD0	AA12	LED1_2	G20	P1_D3N	A17
GMII_TxD1	AB12	LED1_3	H22	P1_D3P	B17
GMII_TxD2	Y11	LED2_0	H21	P2_D0N	A10
GMII_TxD3	AA11	LED2_1	H20	P2_D0P	B10
GMII_TxD4	AB11	LED2_2	J22	P2_D1N	A11
GMII_TxD5	Y10	LED2_3	J21	P2_D1P	B11
GMII_TxD6	AA10	LED3_0	K2	P2_D2N	A12
GMII_TxD7	AB10	LED3_1	K1	P2_D2P	B12
GPIO_0	V3	LED3_2	J3	P2_D3N	A13
GPIO_1	W1	LED3_3	J2	P2_D3P	B13
GPIO_2	W2	LED4_0	J1	P3_D0N	A6
GPIO_3	W3	LED4_1	H3	P3_D0P	B6
ICPU_Addr16	K22	LED4_2	H2	P3_D1N	A7
ICPU_Addr17	K21	LED4_3	H1	P3_D1P	B7
ICPU_Addr18	K20	MDC	AB3	P3_D2N	A8
ICPU_Addr19	L22	MDIO	AA3	P3_D2P	B8

Table 282. Pins by Name *(continued)*

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
P3_D3N	A9	PI_Data6	U21	VDD_8	P15
P3_D3P	B9	PI_Data7	U22	VDD_9	P16
P4_D0N	A2	PI_IRQ_0	AA22	VDD_10	R7
P4_D0P	B2	PI_IRQ_1	AA21	VDD_11	R8
P4_D1N	A3	PI_nCS	W20	VDD_12	R9
P4_D1P	B3	PI_nDone	Y20	VDD_13	R10
P4_D2N	A4	PI_nOE	Y21	VDD_14	R11
P4_D2P	B4	PI_nWR	Y22	VDD_15	R12
P4_D3N	A5	Ref_Filt_0	C22	VDD_16	R13
P4_D3P	B5	Ref_RExt_0	D22	VDD_17	R14
PI_Addr0	T20	Reserved_0	C7	VDD_18	R15
PI_Addr1	T21	Reserved_1	C16	VDD_19	R16
PI_Addr2	T22	Reserved_2	D21	VDD_20	W5
PI_Addr3	R20	Reserved_3	Y2	VDD_21	W6
PI_Addr4	R21	Reserved_4	Y1	VDD_22	W7
PI_Addr5	R22	Reserved_5	D2	VDD_23	W8
PI_Addr6	P20	SI_Clk	AA18	VDD_24	W9
PI_Addr7	P21	SI_DI	Y18	VDD_25	Y4
PI_Addr8	P22	SI_DO	AB19	VDD_26	Y5
PI_Addr9	N20	SI_nEn	AA19	VDD_27	Y6
PI_Addr10	N21	Test_Code0	AA2	VDD_28	Y7
PI_Addr11	N22	Test_Code1	AA1	VDD_29	Y8
PI_Addr12	M20	Test_Code2	Y3	VDD_30	Y9
PI_Addr13	M21	ThermDA	H8	VDD_31	AA4
PI_Addr14	M22	ThermDC	H9	VDD_32	AA5
PI_Addr15	L20	VDD_0	P7	VDD_33	AA6
PI_Addr16	L21	VDD_1	P8	VDD_34	AA7
PI_Data0	W21	VDD_2	P9	VDD_35	AA8
PI_Data1	W22	VDD_3	P10	VDD_36	AA9
PI_Data2	V20	VDD_4	P11	VDD_37	AB4
PI_Data3	V21	VDD_5	P12	VDD_38	AB5
PI_Data4	V22	VDD_6	P13	VDD_39	AB6
PI_Data5	U20	VDD_7	P14	VDD_40	AB7

Table 282. Pins by Name *(continued)*

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
VDD_41	AB8	VDD_A33_19	G19	VDD_IOCPU_6	T4
VDD_42	AB9	VDD_A33_20	H19	VDD_IOCPU_7	T3
VDD_A12_0	H7	VDD_A33_21	N4	VDD_IOCPU_8	T2
VDD_A12_1	H16	VDD_A33_22	N3	VDD_IOCPU_9	T1
VDD_A12_2	J7	VDD_A33_23	N2	VDD_IOCPU_10	R4
VDD_A12_3	J16	VDD_A33_24	N1	VDD_IOCPU_11	R3
VDD_A12_4	K7	VDD_A33_25	M4	VDD_IOCPU_12	R2
VDD_A12_5	K16	VDD_A33_26	M3	VDD_IOCPU_13	R1
VDD_A12_6	L7	VDD_A33_27	M2	VDD_IOCPU_14	P4
VDD_A12_7	L16	VDD_A33_28	M1	VDD_IOCPU_15	P3
VDD_A12_8	M7	VDD_A33_29	L4	VDD_IOCPU_16	P2
VDD_A12_9	M16	VDD_A33_30	L3	VDD_IOCPU_17	P1
VDD_A12_10	N7	VDD_A33_31	L2	VDD_IOMAC_0	W17
VDD_A12_11	N16	VDD_A33_32	L1	VDD_IOMAC_1	W16
VDD_A33_0	D4	VDD_A33_33	K4	VDD_IOMAC_2	W14
VDD_A33_1	D5	VDD_A33_34	J4	VDD_IOMAC_3	W13
VDD_A33_2	D6	VDD_A33_35	H4	VDD_IOMAC_4	W11
VDD_A33_3	D7	VDD_A33_36	G4	VDD_IOMAC_5	W10
VDD_A33_4	D8	VDD_A33_37	G3	VSS_0	F3
VDD_A33_5	D9	VDD_A33_38	G2	VSS_1	C2
VDD_A33_6	D10	VDD_A33_39	G1	VSS_2	B1
VDD_A33_7	D11	VDD_A33_40	F4	VSS_3	C3
VDD_A33_8	D12	VDD_A33_41	E4	VSS_4	C4
VDD_A33_9	D13	VDD_A33_42	E3	VSS_5	C5
VDD_A33_10	D14	VDD_A33_43	E2	VSS_6	C6
VDD_A33_11	D15	VDD_A33_44	E1	VSS_7	C8
VDD_A33_12	D16	VDD_A33_45	D3	VSS_8	C9
VDD_A33_13	D17	VDD_IOCPU_0	L19	VSS_9	C10
VDD_A33_14	D18	VDD_IOCPU_1	M19	VSS_10	C11
VDD_A33_15	D19	VDD_IOCPU_2	P19	VSS_11	C12
VDD_A33_16	D20	VDD_IOCPU_3	R19	VSS_12	C13
VDD_A33_17	E19	VDD_IOCPU_4	U19	VSS_13	C14
VDD_A33_18	F19	VDD_IOCPU_5	V19	VSS_14	C15

Table 282. Pins by Name *(continued)*

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
VSS_15	C17	VSS_40	K8	VSS_63	M15
VSS_16	C18	VSS_41	K9	VSS_64	N8
VSS_17	C19	VSS_42	K10	VSS_65	N9
VSS_18	C20	VSS_43	K11	VSS_66	N10
VSS_19	C21	VSS_44	K12	VSS_67	N11
VSS_20	B22	VSS_45	K13	VSS_68	N12
VSS_21	E21	VSS_46	K14	VSS_69	N13
VSS_22	E22	VSS_47	K15	VSS_70	N14
VSS_23	J19	VSS_48	L8	VSS_71	N15
VSS_26	H10	VSS_49	L9	VSS_IO_0	K19
VSS_27	H11	VSS_50	L10	VSS_IO_1	N19
VSS_28	H12	VSS_51	L11	VSS_IO_2	T19
VSS_29	H13	VSS_52	L12	VSS_IO_3	W19
VSS_30	H14	VSS_53	L13	VSS_IO_4	W18
VSS_31	H15	VSS_54	L14	VSS_IO_5	W15
VSS_32	J8	VSS_55	L15	VSS_IO_6	W12
VSS_33	J9	VSS_56	M8	VSS_IO_7	W4
VSS_34	J10	VSS_57	M9	VSS_IO_8	V4
VSS_35	J11	VSS_58	M10	VSS_IO_9	U4
VSS_36	J12	VSS_59	M11	Xtal1	F2
VSS_37	J13	VSS_60	M12	Xtal2	F1
VSS_38	J14	VSS_61	M13		
VSS_39	J15	VSS_62	M14		

8.3 Pins by Number

This section provides a numeric list of the VSC7395 pins.

Table 283. Pins by Number

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A2	P4_D0N	B14	P1_D0P	D3	VDD_A33_45
A3	P4_D1N	B15	P1_D1P	D4	VDD_A33_0
A4	P4_D2N	B16	P1_D2P	D5	VDD_A33_1
A5	P4_D3N	B17	P1_D3P	D6	VDD_A33_2
A6	P3_D0N	B18	P0_D0P	D7	VDD_A33_3
A7	P3_D1N	B19	P0_D1P	D8	VDD_A33_4
A8	P3_D2N	B20	P0_D2P	D9	VDD_A33_5
A9	P3_D3N	B21	P0_D3P	D10	VDD_A33_6
A10	P2_D0N	B22	VSS_20	D11	VDD_A33_7
A11	P2_D1N	C1	INC_2	D12	VDD_A33_8
A12	P2_D2N	C2	VSS_1	D13	VDD_A33_9
A13	P2_D3N	C3	VSS_3	D14	VDD_A33_10
A14	P1_D0N	C4	VSS_4	D15	VDD_A33_11
A15	P1_D1N	C5	VSS_5	D16	VDD_A33_12
A16	P1_D2N	C6	VSS_6	D17	VDD_A33_13
A17	P1_D3N	C7	Reserved_0	D18	VDD_A33_14
A18	P0_D0N	C8	VSS_7	D19	VDD_A33_15
A19	P0_D1N	C9	VSS_8	D20	VDD_A33_16
A20	P0_D2N	C10	VSS_9	D21	Reserved_2
A21	P0_D3N	C11	VSS_10	D22	Ref_RExt_0
B1	VSS_2	C12	VSS_11	E1	VDD_A33_44
B2	P4_D0P	C13	VSS_12	E2	VDD_A33_43
B3	P4_D1P	C14	VSS_13	E3	VDD_A33_42
B4	P4_D2P	C15	VSS_14	E4	VDD_A33_41
B5	P4_D3P	C16	Reserved_1	E19	VDD_A33_17
B6	P3_D0P	C17	VSS_15	E20	LED0_0
B7	P3_D1P	C18	VSS_16	E21	VSS_21
B8	P3_D2P	C19	VSS_17	E22	VSS_22
B9	P3_D3P	C20	VSS_18	F1	Xtal2
B10	P2_D0P	C21	VSS_19	F2	Xtal1
B11	P2_D1P	C22	Ref_Filt_0	F3	VSS_0
B12	P2_D2P	D1	INC_1	F4	VDD_A33_40
B13	P2_D3P	D2	Reserved_5	F19	VDD_A33_18

Table 283. Pins by Number *(continued)*

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
F20	LED0_3	J7	VDD_A12_2	L2	VDD_A33_31
F21	LED0_2	J8	VSS_32	L3	VDD_A33_30
F22	LED0_1	J9	VSS_33	L4	VDD_A33_29
G1	VDD_A33_39	J10	VSS_34	L7	VDD_A12_6
G2	VDD_A33_38	J11	VSS_35	L8	VSS_48
G3	VDD_A33_37	J12	VSS_36	L9	VSS_49
G4	VDD_A33_36	J13	VSS_37	L10	VSS_50
G19	VDD_A33_19	J14	VSS_38	L11	VSS_51
G20	LED1_2	J15	VSS_39	L12	VSS_52
G21	LED1_1	J16	VDD_A12_3	L13	VSS_53
G22	LED1_0	J19	VSS_23	L14	VSS_54
H1	LED4_3	J20	Clk125_En	L15	VSS_55
H2	LED4_2	J21	LED2_3	L16	VDD_A12_7
H3	LED4_1	J22	LED2_2	L19	VDD_IOCPU_0
H4	VDD_A33_35	K1	LED3_1	L20	PI_Addr15
H7	VDD_A12_0	K2	LED3_0	L21	PI_Addr16
H8	ThermDA	K3	Osc_En	L22	ICPU_Addr19
H9	ThermDC	K4	VDD_A33_33	M1	VDD_A33_28
H10	VSS_26	K7	VDD_A12_4	M2	VDD_A33_27
H11	VSS_27	K8	VSS_40	M3	VDD_A33_26
H12	VSS_28	K9	VSS_41	M4	VDD_A33_25
H13	VSS_29	K10	VSS_42	M7	VDD_A12_8
H14	VSS_30	K11	VSS_43	M8	VSS_56
H15	VSS_31	K12	VSS_44	M9	VSS_57
H16	VDD_A12_1	K13	VSS_45	M10	VSS_58
H19	VDD_A33_20	K14	VSS_46	M11	VSS_59
H20	LED2_1	K15	VSS_47	M12	VSS_60
H21	LED2_0	K16	VDD_A12_5	M13	VSS_61
H22	LED1_3	K19	VSS_IO_0	M14	VSS_62
J1	LED4_0	K20	ICPU_Addr18	M15	VSS_63
J2	LED3_3	K21	ICPU_Addr17	M16	VDD_A12_9
J3	LED3_2	K22	ICPU_Addr16	M19	VDD_IOCPU_1
J4	VDD_A33_34	L1	VDD_A33_32	M20	PI_Addr12

Table 283. Pins by Number *(continued)*

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
M21	PI_Addr13	P16	VDD_9	U3	JTAG_TCK
M22	PI_Addr14	P19	VDD_IOCPU_2	U4	VSS_IO_9
N1	VDD_A33_24	P20	PI_Addr6	U19	VDD_IOCPU_4
N2	VDD_A33_23	P21	PI_Addr7	U20	PI_Data5
N3	VDD_A33_22	P22	PI_Addr8	U21	PI_Data6
N4	VDD_A33_21	R1	VDD_IOCPU_13	U22	PI_Data7
N7	VDD_A12_10	R2	VDD_IOCPU_12	V1	JTAG_TMS
N8	VSS_64	R3	VDD_IOCPU_11	V2	JTAG_TDI
N9	VSS_65	R4	VDD_IOCPU_10	V3	GPIO_0
N10	VSS_66	R7	VDD_10	V4	VSS_IO_8
N11	VSS_67	R8	VDD_11	V19	VDD_IOCPU_5
N12	VSS_68	R9	VDD_12	V20	PI_Data2
N13	VSS_69	R10	VDD_13	V21	PI_Data3
N14	VSS_70	R11	VDD_14	V22	PI_Data4
N15	VSS_71	R12	VDD_15	W1	GPIO_1
N16	VDD_A12_11	R13	VDD_16	W2	GPIO_2
N19	VSS_IO_1	R14	VDD_17	W3	GPIO_3
N20	PI_Addr9	R15	VDD_18	W4	VSS_IO_7
N21	PI_Addr10	R16	VDD_19	W5	VDD_20
N22	PI_Addr11	R19	VDD_IOCPU_3	W6	VDD_21
P1	VDD_IOCPU_17	R20	PI_Addr3	W7	VDD_22
P2	VDD_IOCPU_16	R21	PI_Addr4	W8	VDD_23
P3	VDD_IOCPU_15	R22	PI_Addr5	W9	VDD_24
P4	VDD_IOCPU_14	T1	VDD_IOCPU_9	W10	VDD_IOMAC_5
P7	VDD_0	T2	VDD_IOCPU_8	W11	VDD_IOMAC_4
P8	VDD_1	T3	VDD_IOCPU_7	W12	VSS_IO_6
P9	VDD_2	T4	VDD_IOCPU_6	W13	VDD_IOMAC_3
P10	VDD_3	T19	VSS_IO_2	W14	VDD_IOMAC_2
P11	VDD_4	T20	PI_Addr0	W15	VSS_IO_5
P12	VDD_5	T21	PI_Addr1	W16	VDD_IOMAC_1
P13	VDD_6	T22	PI_Addr2	W17	VDD_IOMAC_0
P14	VDD_7	U1	JTAG_TDO	W18	VSS_IO_4
P15	VDD_8	U2	JTAG_nTRST	W19	VSS_IO_3

Table 283. Pins by Number *(continued)*

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
W20	PI_nCS	Y21	PI_nOE	AA22	PI_IRQ_0
W21	PI_Data0	Y22	PI_nWR	AB2	nReset
W22	PI_Data1	AA1	Test_Code1	AB3	MDC
Y1	Reserved_4	AA2	Test_Code0	AB4	VDD_37
Y2	Reserved_3	AA3	MDIO	AB5	VDD_38
Y3	Test_Code2	AA4	VDD_31	AB6	VDD_39
Y4	VDD_25	AA5	VDD_32	AB7	VDD_40
Y5	VDD_26	AA6	VDD_33	AB8	VDD_41
Y6	VDD_27	AA7	VDD_34	AB9	VDD_42
Y7	VDD_28	AA8	VDD_35	AB10	GMII_TxD7
Y8	VDD_29	AA9	VDD_36	AB11	GMII_TxD4
Y9	VDD_30	AA10	GMII_TxD6	AB12	GMII_TxD1
Y10	GMII_TxD5	AA11	GMII_TxD3	AB13	GMII_GTx_Clk
Y11	GMII_TxD2	AA12	GMII_TxD0	AB14	GMII_RxD7
Y12	GMII_Tx_Er	AA13	MII_Tx_Clk	AB15	GMII_RxD4
Y13	GMII_Tx_En	AA14	GMII_RxD6	AB16	GMII_RxD1
Y14	GMII_RxD5	AA15	GMII_RxD3	AB17	GMII_CRS
Y15	GMII_RxD2	AA16	GMII_RxD0	AB18	GMII_Rx_DV
Y16	GMII_Col	AA17	GMII_Rx_Clk	AB19	SI_DO
Y17	GMII_Rx_Er	AA18	SI_Clk	AB20	ICPU_RxD
Y18	SI_DI	AA19	SI_nEn	AB21	ICPU_PI_En
Y19	ICPU_TxD	AA20	ICPU_SI_Boot_En		
Y20	PI_nDone	AA21	PI_IRQ_1		

9 Package Information

The VSC7395 device is available in the following package types, including lead(Pb)-free packages:

- VSC7395YV is a 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is 0 °C ambient to 100 °C case.
- VSC7395XYV is a lead(Pb)-free, 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is 0 °C ambient to 100 °C case.
- VSC7395YV-03 is a 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is –40 °C ambient to 100 °C case.
- VSC7395XYV-03 is a lead(Pb)-free, 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is –40 °C ambient to 100 °C case.

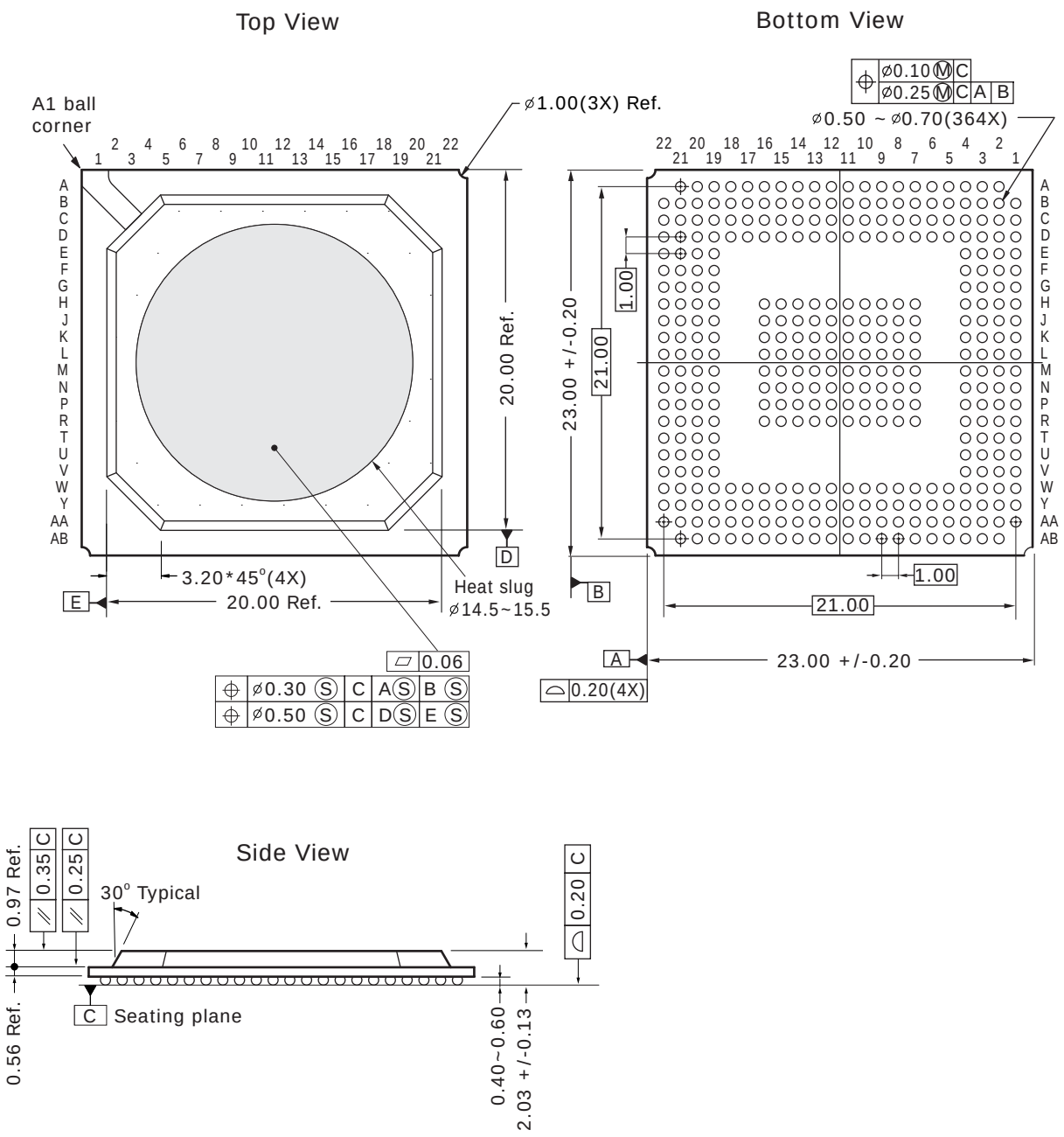
Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC7395 device.

9.1 Package Drawing

The following illustration shows the package drawing for the VSC7395 device. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

Figure 65. Package Drawing



Note:
All dimensions in millimeters.

9.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 284. Thermal Resistances

Part Order Number	θ_{JC}	θ_{JB}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
			0	100	200
VSC7395YV	5.55	9.3	16.1	14.4	13.4
VSC7395XYV	5.55	9.3	16.1	14.4	13.4
VSC7395YV-03	5.55	9.3	16.1	14.4	13.4
VSC7395XYV-03	5.55	9.3	16.1	14.4	13.4

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

9.2.1 Thermal Diode

The VSC7395 device includes an on-die diode that can be used to monitor the die temperature (junction temperature). The operation and accuracy of the diode is not guaranteed and should only be used as a reference.

A thermal sensor, located on the board or in a stand-alone measurement kit, can monitor the die temperature of the switch for thermal management or instrumentation purposes. The following two tables provide the diode parameter and interface specifications. Note that the ThermDC pin is connected to VSS internally in the VSC7395 device.

Notes:

- Vitesse does not support or recommend operation of the thermal diode under reverse bias.
- The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{fw} = I_s \times e^{V_d \times \frac{q}{nkT} - 1}$$

where I_s = saturation current, q = electronic charge, V_d = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin)
The typical value for the diode ideality factor, n, is 1.008.

Table 285. Thermal Diode Interface

Pin Name	Pin Description
ThermDA	Thermal diode anode (p-junction).
ThermDC	Thermal diode cathode (n-junction). Connected to VSS.

9.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

10 Design Guidelines

10.1 Power Supplies

The following guidelines apply to designing power supplies for use with SparX-G5e:

- Make at least one unbroken ground plane (GND).
- Make all the I/O power supply planes unbroken under or over the correlating signals so that the signal return current patterns are unbroken.
- Use the power and ground plane combination as an effective power supply bypass capacitor. The capacitance is proportional to the area of the two planes and inversely proportional to the separation between the planes. Typical values with a 0.25 mm (0.01 inch) separation are 100 pF/in^2. This capacitance is more effective than a capacitor of equivalent value because the planes have no inductance or Equivalent Series Resistance (ESR).
- Do not cut up the power or ground planes in an effort to steer current paths. This usually produces more noise, not less. Furthermore, place vias and clearances in a configuration that maintains the integrity of the plane. Groups of closely spaced vias often overlap clearances. This can form a large slot in the plane. As a result, return currents are forced around the slot. This increases the loop area and therefore EMI emissions. Signals should never be placed on a ground plane because the resulting slot forces return currents around the slot.
- Vias used to connect power planes to the supply and ground balls should be at least 0.25 mm (0.010 inch) in diameter, preferably with no thermal relief, and preferably plated closed with copper or solder. Use separate (or even multiple) vias for each supply and ground ball.

10.1.1 Power Supply Decoupling

Each power supply voltage should have both bulk and high-frequency decoupling capacitors. Recommended capacitors are as follows:

- For bulk decoupling, use 10 µF high capacity and low ESR capacitors or equivalent, distributed across the board.
- For high-frequency decoupling, use 0.1 µF high frequency (for example, X7R) ceramic capacitors placed on the side of the PCB closest to the plane being decoupled, and as close as possible to the power ball. A larger value in the same housing unit produces even better results.
- Use surface mounted components for lower lead inductance and pad capacitance. Smaller form factor components are best (that is, 0402 is better than 0603).

10.1.2 Supply Filtering

Analog supplies should be filtered with a ferrite bead in series with the decoupling capacitors. The capacitor should be located between the ball and the vias to ground plane.

10.2 Clock Configuration

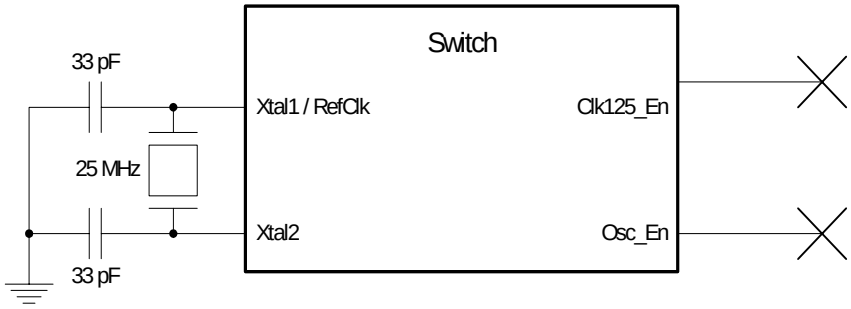
Three different clocking schemes provide the user with design flexibility for a clock strategy.

10.2.1 Crystal Clock Option

A 25-MHz crystal can be connected to the Xtal1 and Xtal2 pins as shown in the following figure. The Osc_En and the Clk125_En pins should be left floating.

Note The figure uses a 33-pF capacitor as an example. The capacitor value varies according to your design or layout requirements.

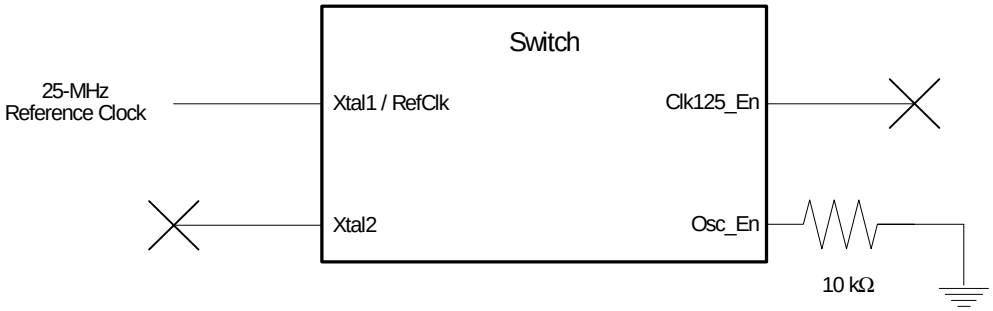
Figure 66. Crystal Clock Option



10.2.2 25-MHz Reference Clock Option

A 25-MHz reference clock can be connected to Xtal1 with Xtal2 left floating. The Osc_En pin needs to be pulled low, and the Clk125_En pin should be left floating as shown in the following figure.

Figure 67. 25-MHz Reference Clock Option

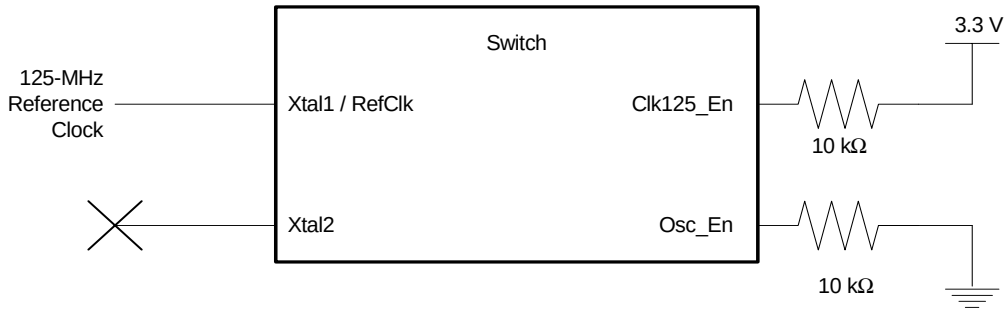


The reference clock must be a low-jitter type and must come from a non-PLL-based clock source (including oscillator, buffer, and so forth). A PLL-based source clock will disturb the built-in PLL.

10.2.3 125-MHz Reference Clock Option

A 125-MHz reference clock can be connected to Xtal1 with Xtal2 left floating. The Osc_En pin needs to be pulled low, and the Clk125_En pin needs to be pulled high as shown in the following figure.

Figure 68. 125-MHz Reference Clock Option



The reference clock must be a low-jitter type and must come from a non-PLL-based clock source (including oscillator, buffer, and so forth). A PLL-based source clock will disturb the built-in PLL.

10.3 Interfaces

10.3.1 General Recommendations

High-speed signals require excellent frequency and phase response up to the third harmonic. The best design would provide excellent frequency and phase response up to the seventh harmonic. The following recommendations can improve signal quality and minimize transmission distances:

- Keep traces as short as possible. Initial component placement should be considered very carefully.
- The impedance of the traces must match the impedance of the termination resistors, connectors, and cable. This reduces reflections due to impedance mismatches.
- Differential impedance must be maintained in a 100-Ω differential application. Routing two 50-Ω traces is not adequate. The two traces must be separated by enough distance to maintain differential impedance.When routing differential pairs, keep the two trace lengths identical. Differences in trace lengths translate directly into signal skew. Note that the differential impedance may be affected when separations occur.
- Keep differential pair traces on the same layer of the PCB to minimize impedance discontinuities.
- Do not group all the passive components together. The pads of the components add capacitance to the traces. At the frequencies encountered, this can result in unwanted reductions in impedance. Use surface mounted 0603 components to reduce this effect.
- Eliminate or reduce stub lengths.
- Reduce or eliminate vias to minimize impedance discontinuities. Remember that vias and their clearance holes in the power and ground plane combination can cause impedance discontinuities in nearby signals.
- Keep signal traces away from other signals, which might capacitively couple noise into the signals. A good rule of thumb is to keep the traces apart by ten times the width of the trace.
- Do not route digital signals from other circuits across the area of the high-speed transmitter and receiver signals.

- Using grounded guard traces is typically not effective for improving signal quality. A ground plane is more effective. However, a common use of guard traces is to route them during the layout, but remove them prior to design completion. This has the benefit of enforcing “Keep-out Areas” around sensitive high-speed signals so that vias and other traces are not accidentally placed incorrectly.
- When signals in a differential pair are mismatched, the result is a common mode current. In a well-designed system, common mode currents should make up less than one percent of the total differential currents. Common mode currents represent a primary source of EMI emissions. To reduce mode currents, route differential traces so that their lengths are the same. For example, a 5 mm (0.2 inch) length mismatch between differential signals having the rise and fall times of 200 ps results in the common mode current being up to 18 % of the differential current.

Notes:

1. Due to the high application frequency, you must be careful to choose proper components (such as the termination resistors) in the designing of the layout of a printed circuit board. The use of surface-mount components is highly recommended to minimize parasitic inductance and lead length of the termination resistor.
2. Matching the impedance of the PCB traces, connectors, and balanced interconnect media is highly recommended. Impedance variations along the entire interconnect path must be minimized because they degrade the signal path and may cause reflections of the signal.

10.3.2 Analog Bias Pins Configuration

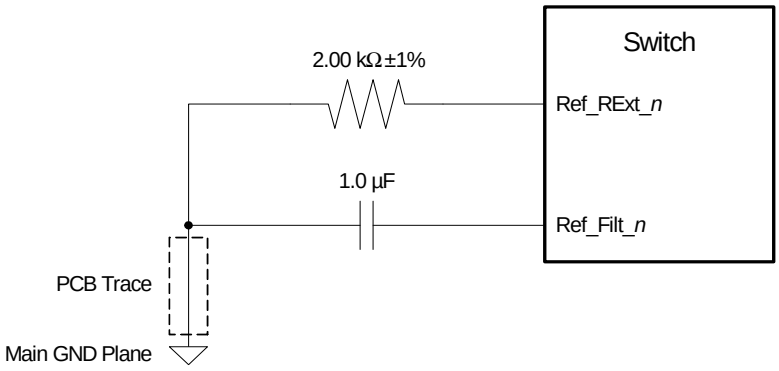
For proper operation, the SparX-G5e device must generate one on-chip band gap reference voltage at the Ref_Filt_0 pins. For this, the following components are required for each SparX-G5e in the system.

- One 2.00 kΩ resistor, ±1%
- One 1 uF capacitor X7R, with 10% tolerance or better

For each of the reference signals, the resistor connects between the Ref_RExt_0 pin and GND. One 1 µF capacitor connects between the Ref_Filt_0 pin and GND.

For best performance, special consideration for the ground connection of the voltage reference circuit is necessary to prevent bus drops, which would cause inaccuracy in the reference voltage. Each of these ground connections should join together at a small common area, and then a short trace should connect this area to the main GND plane as shown in the following figure. All of these components should be placed as close as possible to the SparX-G5e device.

Figure 69. Analog Bias Pins Ground Connection Diagram



10.3.3 MII/GMII/RGMII

The MII/GMII/RGMII signal pins have been designed with fast rise and fall times to allow for 125-MHz operation. To adequately accommodate these signals on a PCB, it is recommended that the traces be designed as either microstrip or stripline transmission lines with a characteristic impedance of 50 Ω. It is also important that an unbroken ground plane exists above and/or below these signals.

For the transmit interface, each pin is self-calibrating to an output impedance of 50 Ω. Thus, external series termination resistors are unnecessary as long as the characteristic impedance of the PCB traces are also 50 Ω.

For the receive interface, careful attention must be paid to the output impedance of the pins on the connected PHY. If that impedance is less than 50 Ω, additional series termination resistors are required. These resistors should be placed as close as possible to the PHY.

If the MII/GMII/RGMII interface is not used, MII_Tx_Clk and GMII_Rx_Clk must be pulled high or low.

10.3.3.1 RGMII Considerations

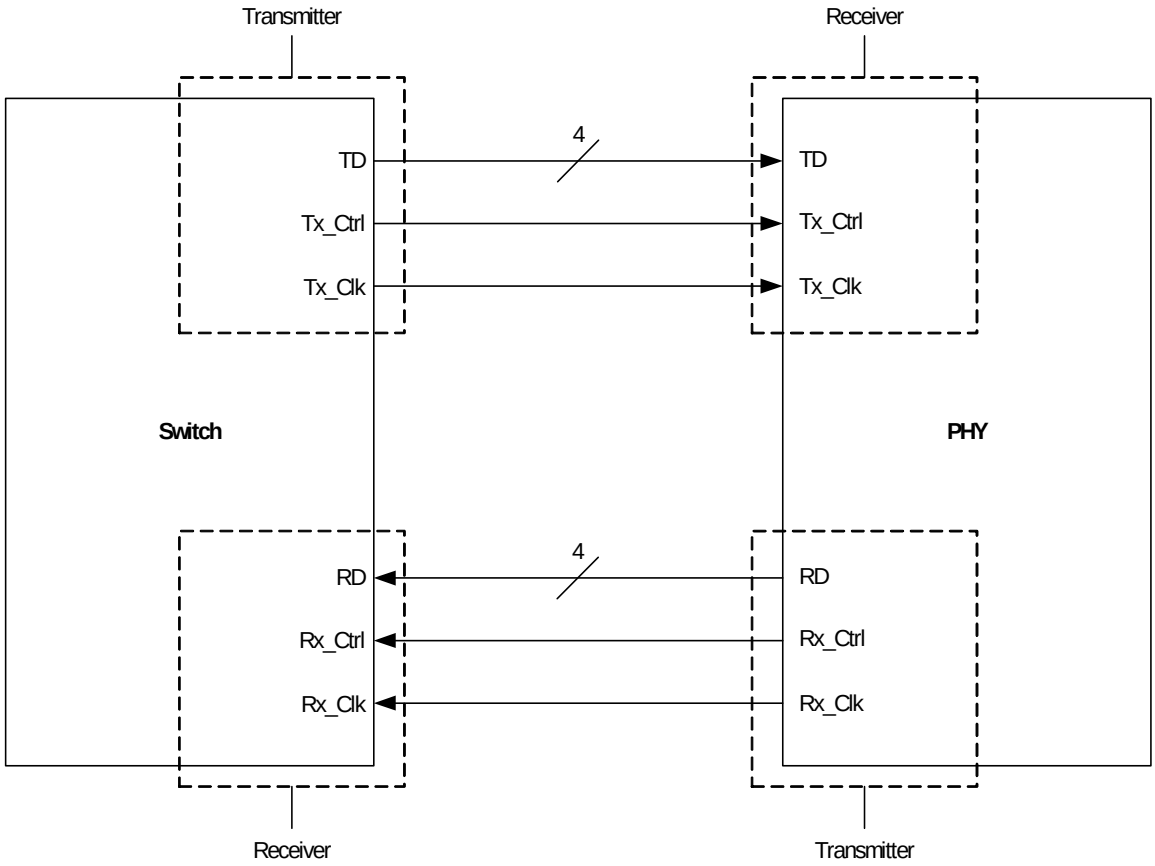
Proper operation of the RGMII bus requires careful control of the timing relationship between clock and data signals.

The RGMII specification requires that the signal clock be delayed by 1/2 bit time (2 ns) at the receiving end of the data path. This clock delay can be added externally (extended clock trace length), or by using internal delays built into the SparX-G5e device.

Clock Delays

When considering the interface between the switch and a PHY, the relationship between transmitter and receiver is often confused. The following figure defines the Rx and Tx interface between the switch and a PHY.

Figure 70. RGMII Receiver (Rx) and Transmitter (Tx) Definitions

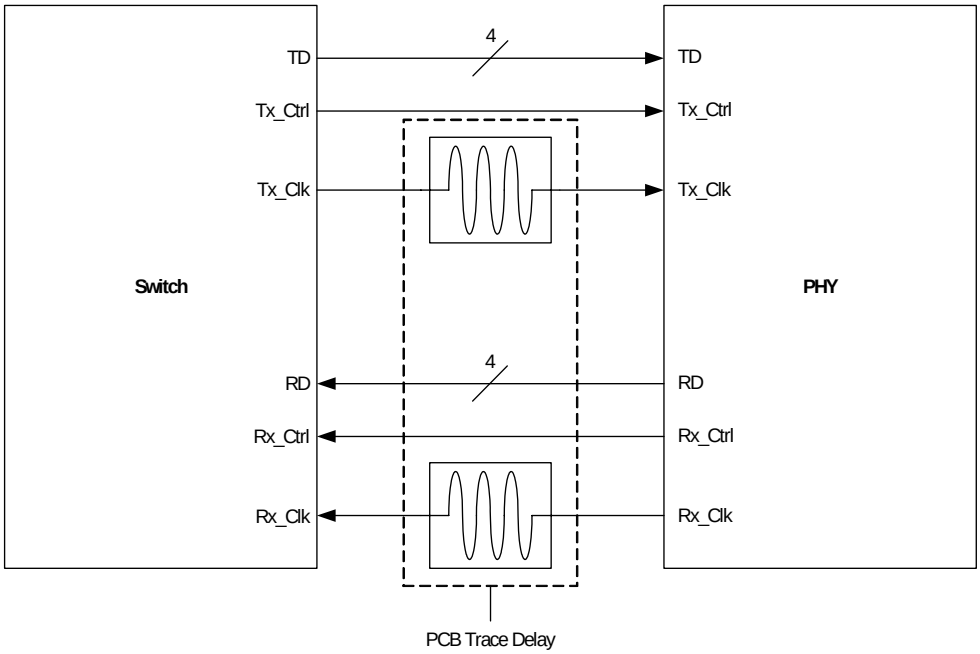


Note that for all traces beginning with Tx, the PHY is the receiver; for all traces beginning with Rx, the switch is the receiver.

There are several methods for the introduction of a clock delay, so that the input registers (receivers) of the switch and PHY see a stable data signal during both rising and falling clock edges.

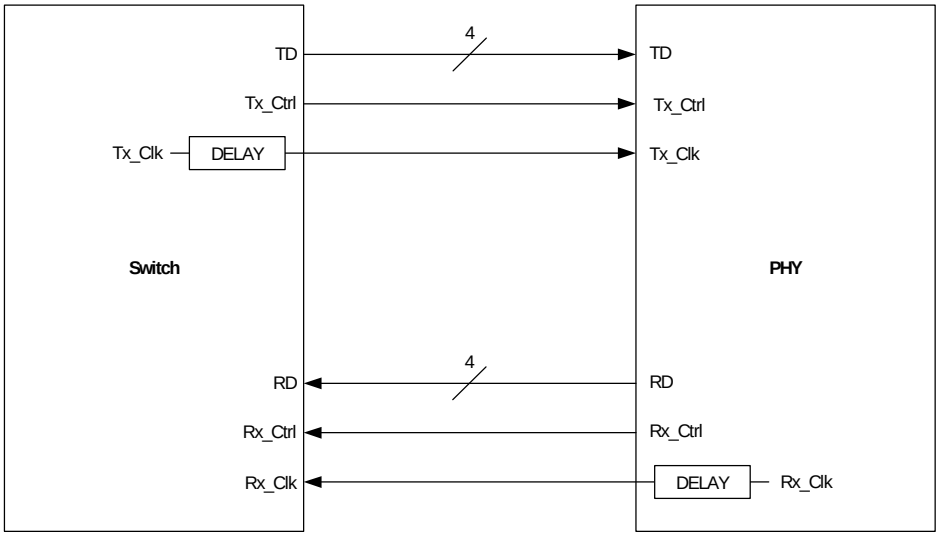
1. A delay of 1.5 ns to 2 ns can be added to the Tx_Clk and Rx_Clk signals by routing them through a long PCB trace delay, as shown in the following figure.

Figure 71. PHY Delay Example



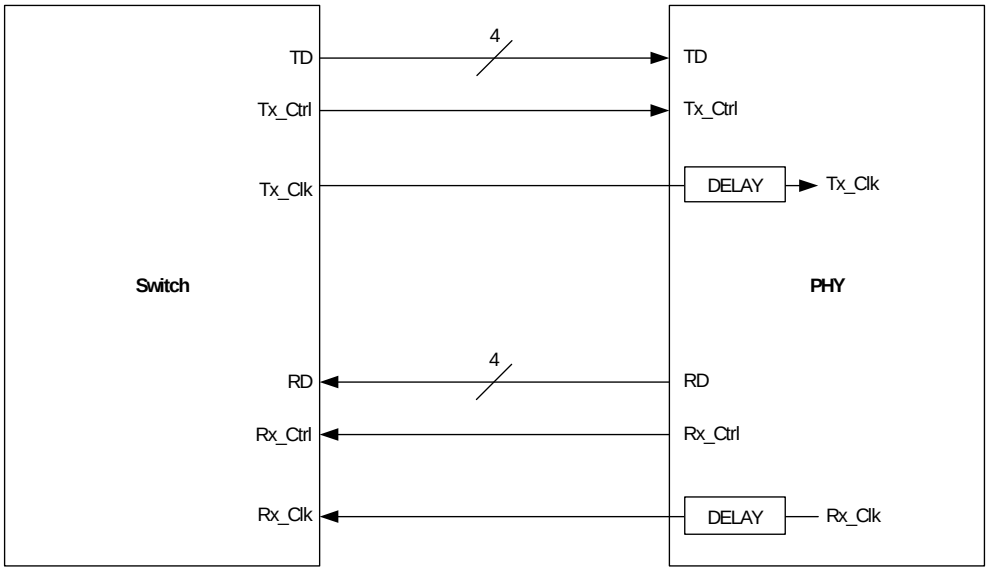
2. An output clock skew can be integrated into the clock signal output of each transmitter. Specifically, this calls for the switch to provide a clock skew on the Tx_Clk; the PHY must provide a clock skew on the Rx_Clk. Devices supporting this type of configuration are defined as RGMII-ID in the RGMII standard.

Figure 72. Cross Delay Example



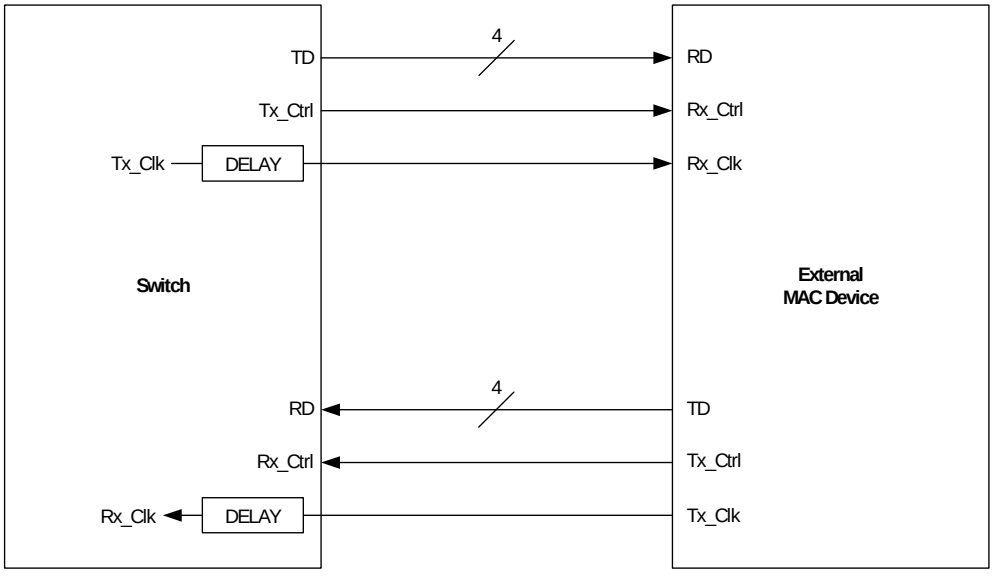
3. A clock skew can be integrated into the PHY for both Rx_Clk and Tx_Clk. Strictly speaking, this method is not compliant with the RGMII standard.

Figure 73. PHY Delay Example



4. When connecting to an external MAC device, the clock skew can integrated into the switch for both Rx_Clk and Tx_Clk.

Figure 74. MAC Delay Example



The SparX-G5e device supports all of the above methods.

Using Integrated Clock Skew to Implement RGMII with SparX-G5e

The SparX-G5e device contains an internal delay element connected to each Tx_Clk and Rx_Clk pin, which can provide the necessary clock delays for the RGMII without the need for PCB trace delays. These elements are enabled in the GMIIDELAY register; for more information, see Table 74, page 151.

When using internal clock skew control, the sets of Tx and Rx traces for each port should be independently matched in length to within one inch (approximately 25 mm). It is not necessary to match the lengths of the Tx traces and the Rx traces on each individual port. A port's Tx traces can be a different length from the port's Rx traces.

10.3.3.2 Reverse MII

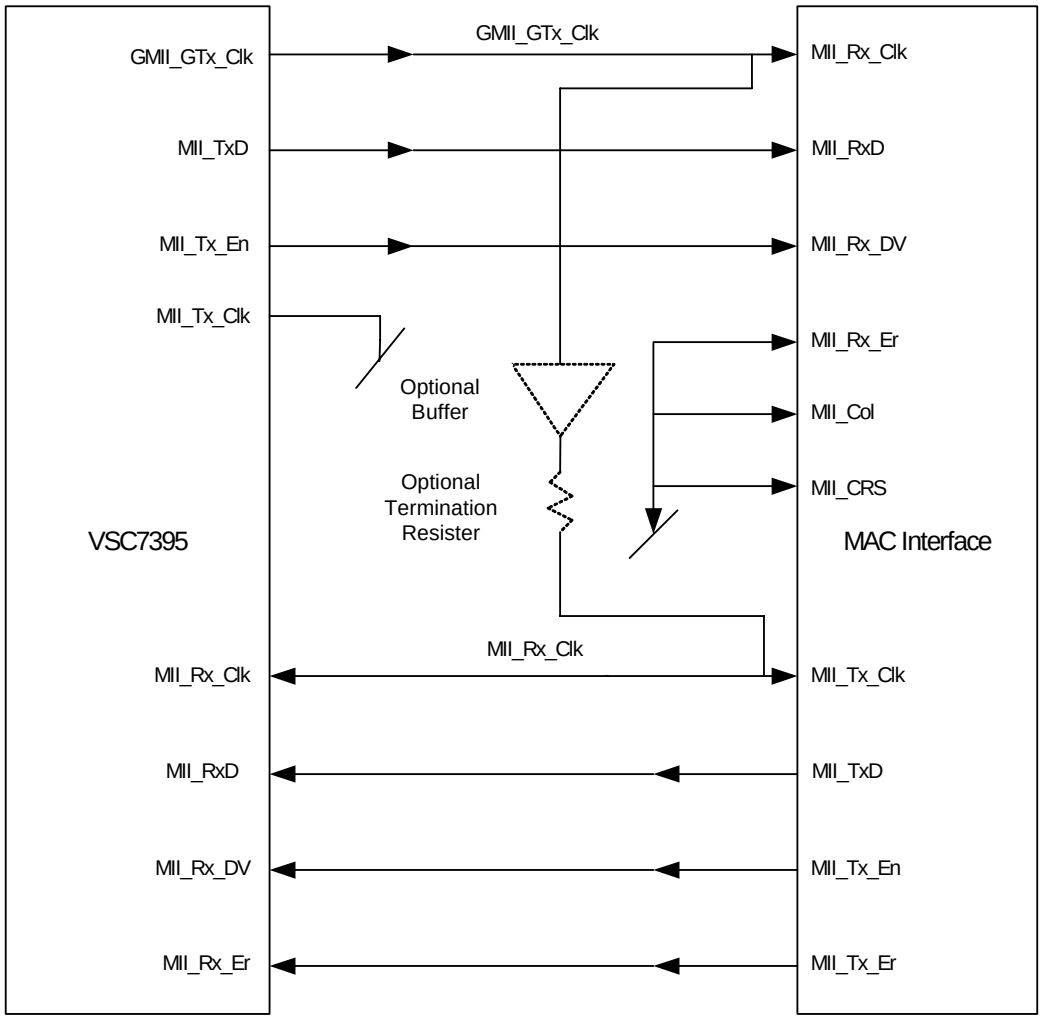
Note Reverse MII can only be used in 10-Mbps or 100-Mbps full-duplex modes.

The MII on the VSC7395 is commonly used as a MAC interface that receives both clocks from the PHY. This can be altered in Reverse MII mode.

For Reverse MII mode, the GMII_GTx_Clk on the VSC7395 can be used as output clock.

To enable GMII_GTx_Clk as the output clock, set the ENABLE_GTX and INVERT_GTX bits in the ADVPORTM register for the port, and connect the interface as shown in the following figure.

Figure 75. Reverse MII Diagram



To set up the reverse MII mode, route the GMII_GTx_Clk from the VSC7395 to the MII_Rx_Clk and the MII_Tx_Clk on the MAC, and back to the MII_Rx_Clk on the VSC7395. This avoids stubs.

Keep the traces short. If this is not possible, fan-out buffers can be placed after the MII_Rx_Clk, and feed buffered clock signals to the MII_Tx_Clk on the MAC and to the MII_Rx_Clk on the VSC7395.

VSC7395 Tx to MAC Rx Timing

For GMII_GTx_Clk falling to MII TxD out, the maximum t_{pd} is 0.5 ns.

The MII_TxD setup to the GMII _GTx_Clk rising clock must be 10 ns according to the MII standard.

One clock cycle at 25 MHz gives 40 ns, with a 60/40 duty cycle; the minimum low period is 16 ns.

The maximum skew between GMII_GTx_Clk is 5.5 ns (16 ns – 10 ns – 0.5 ns), if a setup time of 10 ns is to be fulfilled.

MAC Tx to VSC7395 RxTiming

The setup time from MII_RxD, MII_Rx_DV, MII_Rx_Er, to MII_Rx_Clk rising is minimum 1 ns at the VSC7395 device.

Because both the MAC and the VSC7395 are clocked by the same clock (CGMII_GTx:Clk), the MII_Rx_Clk (MII_Tx_Clk on the MAC) to output delay in the MAC must be bigger than 1 ns. Clock and data may be routed so the traces have equal length from the MAC to the VSC7395.

To ensure that there is a 1 ns delay, the MII_Rx_Clk signal can be routed so it is longer than the data lines from the MAC to the VSC7395.

10.3.4 Twisted-Pair Interface

These pins are the interface to the external Cat5 cable and are organized in four differential pairs for each port. These are labeled Pn_DxP and Pn_DxN, where n is the port number and x is the particular pair within a single interface.

When routing these pairs on a PCB, you must route each pair of positive and negative traces differentially, with a 100 Ω differential characteristic impedance.

10.3.4.1 EMI Designs

Depending on the application (for example, the number of ports, EMI performance requirements such as FCC Class A or B, the quality and type of the equipment shielding, and overall approach to EMI design practice), the twisted-pair interface is designed to be compatible with standard magnetics modules from a wide variety of vendors.

For more information, see the *SparX Magnetic Selection and EMI Control* application note on the Vitesse Web site at www.vitesse.com.

10.3.4.2 Transmit Amplitude Measurement and IEEE Compliance Testing

When making transmit amplitude measurements, consider the following matters carefully:

- The integrated PHYs are optimized for lowest power, so the measured transmit amplitude, while still meeting all IEEE requirements, can sometimes be in the lower range of the specification.
- The measurement requires very precise measurement techniques and carefully calibrated equipment.

For more information about the transmit amplitude measurement and IEEE compliance testing, contact your Vitesse Field Applications Engineer.

10.3.5 PI

This section applies when the parallel interface is enabled.

The parallel interface (PI) consists of PI_Addr[16:0], PI_Data[7:0], PI_nCS, PI_nDone, PI_nOE, PI_nWR, and PI_IRQ_[1:0]. If this interface is not used, all signals can be left floating.

When using the parallel interface, note that the timing parameter, $t_{d(SLNH)}$, indicates when an issued command is sampled by SparX-G5e. For more information about this timing parameter, see "AC Specifications for PI," page 237.

To ensure that the PI_nDone signal is driven inactive properly, add a 4.7-kΩ pull-up resistor to this signal.

10.3.6 SI

If the serial CPU interface is not used, all input signals can be left floating.

The SI bus consists of the SI_Clk clock signal, the SI_DO and SI_DI data signals, and the SI_nEN device select signal.

When routing the SI_Clk signal, be sure to create clean edges. If the SI bus is connected to more than one slave device, it should be routed in a daisy chain configuration with no stubs. The SI_Clk signal should be terminated correctly to avoid reflections and double clocking.

If it is not possible (or desirable) to route the bus in a daisy chain configuration, the SI_Clk signal should be buffered and routed in a star topology from the buffers. Each buffered clock should be terminated at its source.

10.4 JTAG

If the JTAG interface is not used, nTRST must be pulled to GND to reset the JTAG controller. This is also required during normal operation.

The signals TMS, TDI, and TCK have an internal built-in pull up resistor.

10.5 GPIO

The GPIO_[3:0] pins are designed to provide a current sourcing and sinking capability, as specified in Table 238, page 220. For more information, see "DC Specifications for PI, V-Core CPU, SI, JTAG, and Other Control Signals," page 219.

GPIOs are typically used to control status LEDs. The GPIOs provide a limited current sourcing and sinking capability; therefore, Vitesse recommends that you consider the use of high-effeciency LEDs.

10.6 Pull Resistors

All single-ended inputs on SparX-G5e that are unused and do not have a built-in pull resistor must have an external pull resistor to maintain a stable level. For information about the pull information for each signal, see "Pins by Function," page 252.

Note Remember to pull the Reserved_x pins according to the values given in Table 281, page 262.

10.7 V-Core CPU Flash Access

When selecting an external flash for the V-Core CPU, the clock frequency of the V-Core CPU must be taken into consideration, because during a read operation, ICPU_ROM_nCS is low for two 8051 clock cycles. For more information about the timing, see "V-Core CPU ROM/Flash Read," page 241 .

The following table illustrates the timing restrictions focusing on time left for the flash access for a 17.36-MHz and a 26.04-MHz V-Core CPU clock frequency.

Table 286. Flash Access Timing

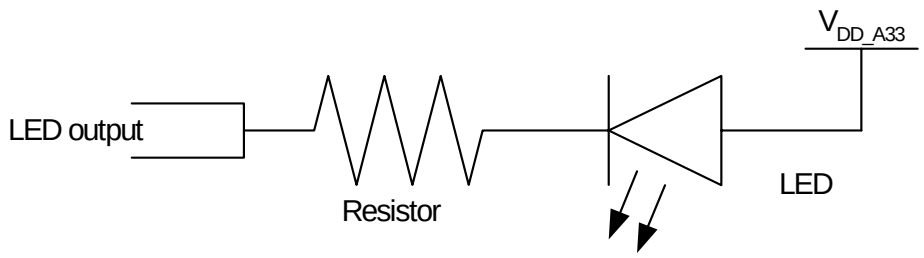
Timing	Clock Frequency 17.36 MHz	Clock Frequency 26.04 MHz	Unit
ICPU_ROM_nCS active (2 V-Core CPU clock cycles)	115	77	ns
Data setup time before ICPU_ROM_nCS goes inactive with IPU_ROM_CFG::CS_RD_DELAY set to 0 ns	20	20	ns
Board delay (traces)	2	2	ns
Time left for flash access	115 – 20 – 2 = 93	77 – 20 – 2 = 55	ns

Therefore, running the V-Core CPU at 17.36 MHz (divide with 9) requires a flash with a 90 ns access time, and running the V-Core CPU at 26.04 MHz (divide with 6) requires a flash with a 45 ns access time.

10.8 LED Outputs

All LED outputs are active-low. LEDs should be driven from the VDD_A33 power supply through a limiting resistor as shown in the following figure.

Figure 76. Driving LEDs Through a Limiting Resistor



11 Design Considerations

This section provides information about the design considerations for the VSC7395 device.

11.1 Mirroring Might Cause Drop on Mirrored Ports

Issue

Two ports transmitting to each other at 100% load and both mirroring to a third port, can experience up to 1% frame drop. The drop rate is highest for 64-byte frame sizes. There are no drops for 1518-byte frame sizes.

Workaround

No workaround exists.

Status

There are currently no plans to fix this erratum.

12 Ordering Information

The VSC7395 device is available in the following package types, including lead(Pb)-free packages:

- VSC7395YV is a 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is 0 °C ambient to 100 °C case.
- VSC7395XYV is a lead(Pb)-free, 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is 0 °C ambient to 100 °C case.
- VSC7395YV-03 is a 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is –40 °C ambient to 100 °C case.
- VSC7395XYV-03 is a lead(Pb)-free, 364-pin, thermally enhanced, plastic ball grid array (BGA) with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is –40 °C ambient to 100 °C case.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC7395 device.

Table 287. Ordering Information

Part Order Number	Description
VSC7395YV	364-pin, thermally enhanced, plastic BGA with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is 0 °C ambient to 100 °C case.
VSC7395XYV	Lead(Pb)-free, 364-pin, thermally enhanced, plastic BGA with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is 0 °C ambient to 100 °C case.
VSC7395YV-03	364-pin, thermally enhanced, plastic BGA with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is –40 °C ambient to 100 °C case.
VSC7395XYV-03	Lead(Pb)-free, 364-pin, thermally enhanced, plastic BGA with a 23 mm × 23 mm body size, 1 mm pin pitch, and 2.16 mm maximum height. The operating temperature is –40 °C ambient to 100 °C case.